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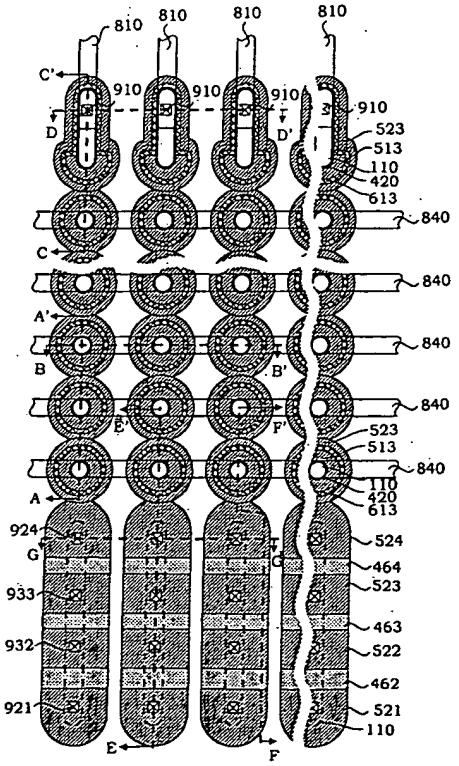
## (54) A semiconductor memory and its production process

(57) A semiconductor memory comprises: a first conductivity type semiconductor substrate and one or more memory cells constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer, wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate.

Fig. 1

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## Description

### BACKGROUND OF THE INVENTION

1.Field of the Invention

**[0001]** The present invention relates to a semiconductor memory and its production process, and more particularly, the invention relates to a semiconductor memory provided with a memory transistor having a charge storage layer and a control gate, and its production process.

2.Description of Related Art

**[0002]** As a memory cell of an EEPROM, is known a device of a MOS transistor structure having a charge storage layer and a control gate in a gate portion, in which an electric charge is injected into and released from the charge storage layer by use of a tunnel current. In this memory cell, data "0" and "1" is stored as changes in a threshold voltage by the state of the charge in the charge storage layer. For example, in the case of an n-channel memory cell using a floating gate as the charge storage layer, when a source/drain diffusion layer and a substrate are grounded and a high positive voltage is applied to the control gate, electrons are injected from the substrate into the floating gate by a tunnel current. This injection of electrons shifts the threshold voltage of the memory cell toward positive. When the control gate is grounded and a high positive voltage is applied to the source/drain diffusion layer or the substrate, electrons are released from the floating gate to the substrate by the tunnel current. This release of electrons shifts the threshold voltage of the memory cell toward negative.

**[0003]** In the above-described operation, a relationship of capacity coupling between the floating gate and the control gate with capacity coupling between the floating agate and the substrate plays an important role in effective injection and release of electrons, i.e., effective writing and erasure. That is, the larger the capacity between the floating gate and the control gate, the more effectively the potential of the control gate can be transmitted to the floating gate and the easier the writing and erasure become.

**[0004]** With recent development in semiconductor technology, especially, in micro-patterning techniques, the size reduction and the capacity increase of memory cells of EEPROM are rapidly progressing. Accordingly, it is an important how large capacity can be ensured between the floating gate and the control gate.

**[0005]** For increasing the capacity between the floating gate and the control gate, it is necessary to thin a gate insulating film therebetween, to increase the dielectric constant of the gate insulating film or to enlarge an area where the floating gate opposes the control gate.

**[0006]** However, the thinning of the gate insulating film is limited in view of reliability of memory cells. For increasing the dielectric constant of the gate insulating film, a silicon nitride film is used as the gate insulating film instead of a silicon oxide film. This is also questionable in view of reliability and is not practical. Therefore, in order to ensure a sufficient capacity between the floating gate and the control gate, it is necessary to set a sufficient overlap area therebetween. This is, however, contradictory to the size reduction of memory cells and the capacity increase of EEPROM.

**[0007]** In an EEPROM disclosed by Japanese Patent No.2877462, memory transistors are formed by use of sidewalls of a plurality of pillar-form semiconductor layers arranged in matrix on a semiconductor substrate, the pillar-form semiconductor layers being separated by trenches in a lattice form. A memory transistor is composed of a drain diffusion layer formed on the top of a pillar-form semiconductor layer, a common source diffusion layer formed at the bottom of the trenches, and a charge storage layer and a control gate which are around all the periphery of the sidewall of the pillar-form semiconductor layer. The control gates are provided continuously for a plurality of pillar-form semiconductor layers lined in one direction so as to form a control gate line, and a bit line is connected to drain diffusion layers of a plurality of memory transistors lined in a direction crossing the control gate line. The charge storage layer and the control gate are formed in a lower part of the pillar-form semiconductor layer. This construction can prevent a problem in a one transistor/one cell structure, that is, if a memory cell is over-erased (a reading potential is 0 V and the threshold is negative), a cell current flows in the memory cell even if it is not selected.

**[0008]** With this construction, a sufficiently large capacity can be ensured between the charge storage layer and the control gate with a small area occupied. The drain regions of the memory cells connected to the bit lines are formed on the top of the pillar-form semiconductor layers and completely insulated from each other by the trenches. A device isolation region can further be decreased and the memory cells are reduced in size. Accordingly, it is possible to obtain a mass-storage EEPROM with memory cells which provide excellent writing and erasing efficiency.

**[0009]** The prior-art EEPROM is explained with reference to figures. Fig. 800 is a plan view of a prior-art EEPROM, and Figs. 801(a) and 801(b) are sectional views taken on lines A-A' and B-B', respectively, in Fig. 800.

**[0010]** In Fig. 800, pillar-form silicon semiconductor layers 2 are columnar, that is, the top thereof is circular. However, the shape of the pillar-form silicon semiconductor layers need not be columnar. In the plan view of Fig. 800, selection gate lines formed by continuing gate electrodes of selection gate transistors are not shown for avoiding complexity of the figure.

**[0011]** In the prior art, is used a P-type silicon substrate 1, on which a plurality of pillar-form P-type silicon layers 2 are arranged in matrix. The pillar-form P-type

silicon layers 2 are separated by trenches 3 in a lattice form and functions as memory cell regions. Drain diffusion layers 10 are formed on the top of the silicon layers 2, common source diffusion layers 9 are formed at the bottom of the trenches 3, and oxide films 4 are buried at the bottom of the trenches 3. Floating gates 6 are formed in a lower part of the silicon layers 2 with intervention of tunnel oxide films 5 so as to surround the silicon layers 2. Outside the floating gates 6, control gates 8 are formed with intervention of interlayer insulating films 7. Thus memory transistors are formed. Here, as shown in Figs. 800 and 801(b), the control gates 8 are provided continuously for a plurality of memory cells in one direction so as to form control gate lines (CG1, CG2, ...). Gate electrodes 32 are provided around an upper part of the silicon layers 2 with intervention of gate oxides films 31 to form the selection gate transistors, like the memory transistors. The gate electrodes 32 of the selection gate transistors, like the control gates 8 of the memory cells, are provided continuously in the same direction as that of the control gates 8 of the memory cells so as to form selection gate lines, i.e., word lines WL (WL1, WL2, ...).

**[0012]** Thus, the memory transistors and the selection gate transistors are buried in the trenches in a stacked state. The control gate lines leave end portions as contact portions 14 on the surface of silicon layers, and the selection gate lines leaves contact portions 15 on silicon layers on an end opposite to the contact portions 14 of the control gates. Al wires 13 and 16 to be control gate lines CG and the word lines WL, respectively, are contacted to the contact portion 14 and 15, respectively. At the bottom of the trenches 3, common source diffusion layers 9 of the memory cells are formed, and on the top of the silicon layers 2, drain diffusion layers 10 are formed for every memory cell. The resulting substrate with the thus formed memory cells is covered with a CVD oxide film 11, where contact holes are opened. Al wires 12 are provided which are to be bit lines BL which connects the drain diffusion layers 10 of memory cells lined in a direction crossing the word lines WL. When patterning is carried out for the control gate lines, a mask is formed of PEP on pillar-form silicon layers at an end of a cell array to leave, on the surface of the silicon layers, the contact portions 14 of a polysilicon film which connect with the control gate lines. To the contact portions 14, the Al wires 13 which are to be control gate lines are contacted by Al films formed simultaneously with the bit lines BL.

**[0013]** A production process for obtaining the structure shown in Fig. 801(a) is explained with reference to Figs. 801(a) to 805(g). A P-type silicon layer 2 with a low impurity concentration is epitaxially grown on a P-type silicon substrate 1 with a high impurity concentration to give a wafer. A mask layer 21 is deposited on the wafer and a photoresist pattern 22 is formed by a known PEP process. The mask layer 21 is etched using the photoresist pattern 22 (see Fig. 802(a)).

**[0014]** The silicon layer 2 is etched by a reactive ion etching method using the resulting mask layer 21 to form trenches 3 in a lattice form which reach the substrate. Thereby the silicon layer 21 is separated into a plurality of pillar-form islands. A silicon oxide film 23 is deposited by a CVD method and anisotropically etched to remain on the sidewalls of the pillar-form silicon layers 2. By implantation of N-type impurity ions, drain diffusion layers 10 are formed on the top of the pillar-form silicon layers 2 and common source diffusion layers 9 are formed at the bottom of the trenches (see Fig. 802(b)).

**[0015]** The oxide films 23 around the pillar-form silicon layers 2 are etched away by isotropic etching. Channel ion implantation is carried out on the sidewalls of the pillar-form silicon layers 2 by use of a slant ion implantation as required. Instead of the channel ion implantation, an oxide film containing boron may be deposited by a CVD method with a view to utilizing diffusion of boron from the oxide film. A silicon oxide film 4 is deposited by a CVD method and isotropically etched to be buried at the bottom of trenches 3. Tunnel oxide films 5 are formed to a thickness of about 10 nm around the silicon layers 2 by thermal oxidation. A first-layer polysilicon film 5 is deposited and anisotropically etched to remain on lower sidewalls of the pillar-form silicon layers 2 as floating gates 6 around the silicon layers 2 (see Fig. 803 (c)).

**[0016]** Interlayer insulating films 7 are formed on the surface of the floating gates 5 formed around the pillar-form silicon layers 2. The interlayer insulating films 7 are formed of an ONO film, for example. The ONO film is formed by oxidizing the surface of the floating gate 6 by a predetermined thickness, depositing a silicon nitride film by a plasma-CVD method and then thermal-oxidizing the surface of the silicon nitride film. A second-layer polysilicon film is deposited and anisotropically etched to form control gates 8 on lower parts of the pillar-form silicon layers 2 (see Fig. 803(d)). At this time, the control gates 8 are formed as control gate lines continuous in a longitudinal direction in Fig. 800 without need to perform a masking process by previously setting intervals between the pillar-form silicon layers 2 in the longitudinal direction at a predetermined value or less. Unnecessary parts of the interlayer insulating films 7 and underlying tunnel oxide films 2 are etched away. A silicon oxide film 111 is deposited by a CVD method and etched halfway down the trenches 3, that is, to a depth such that the floating gates 6 and control gates 8 of the memory cells are buried and hidden (see Fig. 804(e)).

**[0017]** A gate oxide film 31 is formed to a thickness of about 20 nm on exposed upper parts of the pillar-form silicon layers 2 by thermal oxidation. A third-layer polysilicon film is deposited and anisotropically etched to form gate electrodes 32 of MOS transistors (see Fig. 804(f)). The gate electrodes 32 are patterned to be continuous in the same direction as the control gate lines run, and form selection gate lines. The selection gate lines can be formed continuously in self-alignment, but

this is more difficult than the control gates 8 of the memory cells. For, the selection gate transistors are single-layer gates while the memory transistors are two-layered gates, and therefore, the intervals between adjacent selection gates are wider than the intervals between the control gates. Accordingly, in order to ensure that the gate electrodes 32 are continuous, the gate electrodes may be formed in a two-layer polysilicon structure, a first polysilicon film may be patterned to remain only in locations to connect the gate electrodes by use of a masking process, and a second polysilicon film may be left on the sidewalls.

**[0018]** Masks for etching the polysilicon films are so formed that contact portions 14 and 15 of the control gate lines and the selection gate lines are formed on the top of the pillar-form silicon layers at different ends. A silicon oxide film 112 is deposited by a CVD method and, as required, is flattened. Contact holes are opened. An Al film is deposited and patterned to form Al wires 12 to be bit lines BL, Al wires 13 to be control gate lines CG and Al wires 16 to be word lines WL at the same time (see Fig. 805(g)).

**[0019]** Fig. 806(a) schematically shows a sectional structure of a major part of one memory cell of the prior-art EEPROM, and Fig. 806(b) shows an equivalent circuit of the memory cell. The operation of the prior-art EEPROM is briefly explained with reference to Figs. 806 (a) to 806(b).

**[0020]** For writing by use of injection of hot carriers, a sufficiently high positive potential is applied to a selected word line WL, and positive potentials are applied to a selected control gate line CG and a selected bit line BL. Thereby, a positive potential is transmitted to the drain of a memory transistor Qc to let a channel current flow in the memory transistor Qc and inject hot carriers. Thereby, the threshold of the memory cell is shifted toward positive. For erasure, 0 V is applied to a selected control gate CG and high positive potentials are applied to the word line WL and the bit line BL to release electrons from the floating gate to the drain. For erasing all the memory cells, a high positive potential may be applied to the common sources to release electrons to the sources. Thereby, the thresholds of the memory cells are shifted toward negative. For reading, the selection gate transistor is rendered ON by the word line WL and the reading potential is applied to the control gate line CG. The judgement of a "0" or a "1" is made from the presence or absence of a current.

**[0021]** In the case where an FN tunneling is utilized for injecting electrons, high potentials are applied to a selected control gate line CG and a selected word line WL and 0 V is applied to a selected bit line BL to inject electrons from the substrate to the floating gate.

**[0022]** This prior art provides an EEPROM which does not mis-operate even in an over-erased state thanks to the presence of the selection gate transistors.

**[0023]** The prior-art EEPROM does not have diffusion layers between the selection gate transistors Qs and the memory transistors Qc as shown in Fig. 806(a). For, it is hard to form the diffusion layers selectively on the sidewalls of the pillar-form silicon layers. Therefore, in the structure shown in Figs. 801(a) and 801(b), desirably, separation oxide films between the gates of the memory transistors and the gates of the selection gate transistors are as thin as possible. In the case of utilizing the injection of hot electrons, in particular, the separation oxide films need to be about 30 to 40 nm thick for allowing a sufficient "H" level potential to be transmitted to the drain of a memory transistor. Such fine intervals cannot be practically made only by burying the oxide films by the CVD method as described above in the production process. Accordingly, desirably, the oxide films are buried in such a manner that the floating gates 6 and the control gates 8 are exposed, and thin oxide films are formed on exposed parts of the floating gates 6 and the control gates 8 simultaneously with the formation of the gate oxide films for the selection gate transistors.

**[0024]** Further, according to the prior art, since the pillar-form silicon layers are arranged with the bottom of the lattice-form trenches forming an isolation region and the memory cells are constructed to have the floating gates formed to surround the pillar-form silicon layers, it is possible to obtain a highly integrated EEPROM in which the area occupied by the memory cells are small. Furthermore, although the memory cells occupy a small area, the capacity between the floating gates and the control gates can be ensured to be sufficiently large.

**[0025]** According to the prior art, the control gates of the memory cells are formed to be continuous in one direction without using a mask. This is possible, however, only when the pillar-form silicon layers are arranged at intervals different between a longitudinal direction and a lateral direction. That is, by setting the intervals between adjacent pillar-form silicon layers in a word line direction to be smaller than the intervals between adjacent pillar-form silicon layers in a bit line direction, it is possible to obtain control gate lines that are separated in the bit line direction and are continuous in the word line direction automatically without using a mask.

**[0026]** In contrast, when the pillar-form silicon layers are arranged at the same intervals both in the longitudinal direction and in the lateral direction, a PEP process is required. More particularly, the second-layer polysilicon film is deposited thick, and through the PEP process to form a mask, the second-layer polysilicon film is selectively etched to remain in locations to be continuous as control gate lines. The third-layer polysilicon film is deposited and etched to remain on the sidewalls as described regarding the production process of the prior art. Even in the case where the pillar-form silicon layers are arranged at intervals different between the longitudinal direction and the lateral direction, the continuous control gate lines cannot be automatically formed depending upon the intervals of the pillar-form silicon layers. In this case, the mask process by the PEP process as described above can be used for forming the control gate

lines continuous in one direction.

**[0027]** Although the memory cells of the prior art as described above are of a floating gate structure, the charge storage layers do not necessarily have the floating gate structure and may have a structure such that the storage of a charge is realized by a trap in a laminated insulating film, e.g., a MNOS structure.

**[0028]** Fig. 807 is a sectional view of a prior-art memory with memory cells of the MNOS structure, corresponding to Fig. 801(a). A laminated insulating film 24 functioning as the charge storage layer is of a laminated structure of a tunnel oxide film and a silicon nitride film, or of a tunnel oxide film, a silicon nitride film and further an oxide film formed on the silicon nitride film.

**[0029]** Fig. 808 is a sectional view of a prior-art memory in which the memory transistors and the selection gate transistors of the above-described prior art are exchanged, i.e., the selection gate transistors are formed in the lower parts of the pillar-form silicon layers 2 and the memory transistors are formed in the upper parts of the pillar-form silicon layers 2. Fig. 808 corresponds to Fig. 801(a). This structure in which the selection gate transistors are provided on a common source side can apply to the case where the injection of hot electrons is used for writing.

**[0030]** Fig. 809 shows a prior-art memory in which a plurality of memory cells are formed on one pillar-form silicon layer. Like numbers denote like components in the above-described prior-art memories and the explanation thereof is omitted.

**[0031]** In this memory, a selection gate transistor Qs1 is formed in the lowermost part of a pillar-form silicon layer 2, three memory transistors Qc1, Qc2 and Qc3 are laid above the selection gate transistor Qs1, and another selection gate transistor Qs2 is formed above. This structure can be obtained basically by repeating the aforesaid production process.

**[0032]** As described above, the prior-art techniques can provide highly integrated EEPROMs whose control gates and charge storage layers have a sufficient capacity therebetween and whose memory cells occupy a decreased area, by constructing the memory cells using memory transistors having the charge storage layers and the control gates by use of the sidewalls of the pillar-form semiconductor layers separated by the lattice-form trenches.

**[0033]** However, if a plurality of memory cells are connected in series on one pillar-form semiconductor layer and the thresholds of the memory cells are supposed to be the same, significant changes take place in the thresholds of memory cells at both ends of the memory cells connected in series owing to a back-bias effect of the substrate in a reading operation. In the reading operation, the reading potential is applied to the control gate lines CG and the "0" or "1" is judged from the presence of a current. For this reason, the number of memory cells connected in series is limited in view of the performance of memories. Therefore, the production of mass-storage memories is difficult to realize.

**[0034]** The problem that the thresholds of memory cells are changed owing to a back-bias effect is true not only of the case where a plurality of memory cells are connected in series on one pillar-form semiconductor layer but also of the case where one memory cell is formed on one pillar-form semiconductor, depending upon variations in the back-bias effect of the substrate in an inplanar direction.

**[0035]** In the prior art memory, an impurity diffusion layer is not formed between memory cells on the same pillar-form semiconductor layer. However, it is preferable that an impurity diffusion layer is formed therebetween.

**[0036]** Furthermore, in the prior-art memories, the charge storage layers and the control gates are formed in self-alignment with the pillar-form semiconductor layers. Taking mass storage of the cell array into consideration, the pillar-form semiconductor layers are preferably formed at the minimum photoetching dimension.

**[0037]** In the case where the floating gates are used as the charge storage layers, the capacity coupling between the floating gates and the control gates and between the floating gates and the substrate is determined by the area of the outer periphery of the pillar-form semiconductor layers, the area of the outer periphery of the floating gate, the thickness of the tunnel oxide films insulating the floating gates from the pillar-form semiconductor layers and the thickness of the interlayer insulating films insulating the floating gates form the control gates. In the prior-art memories, the charge storage layers and the control gates are formed to surround the pillar-form semiconductor layers by utilizing the sidewalls of the pillar-form semiconductor layers in order that the capacity between the charge storage layers and the control gates is ensured to be sufficiently large. However, in the case where the pillar-form semiconductor layers are formed at the minimum photoetching dimension and the thickness of the tunnel oxide films and that of the interlayer insulating film are fixed, the capacity between the charge storage layers and the control gates is determined simply by the area of the outer periphery of the floating gates, that is, the thickness of the floating gates. Therefore, it is difficult to increase the capacity between the charge storage layers and the control gates without increasing the area occupied by the memory cells. In other words, it is difficult to increase the ratio of the capacity between the floating gates and the control gates to the capacity between the floating gates and the pillar-form semiconductor layers without increasing the area occupied by the memory cells.

**[0038]** Further, if transistors are formed in a direction vertical to the substrate stage by stage, there occur variations in characteristics of the memory cells owing to differences in the properties of the tunnel oxide films and differences in the profile of diffusion layers. Such differences are generated by thermal histories different stage by stage.

## SUMMARY OF THE INVENTION

**[0039]** The present invention has been made in view of the above-mentioned problems. An object of the invention is to provide a semiconductor memory and a production process therefor, in which the degree of integration of the memory is improved by reducing the back-bias effect in a semiconductor memory having charge storage layers and control gates, capacity between the floating gates and the control gates is increased without increasing the occupied area and variations in the characteristics of memory cells are suppressed.

**[0040]** The present invention provides a semiconductor memory comprising:

a fist conductivity type semiconductor substrate and one or more memory cells constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate.

**[0041]** The present invention also provides a process for producing a semiconductor memory having at least one memory cell constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;
forming an insulating film and a first conductive film over a surface of the island-like semiconductor layer;
forming sidewall spacers of an insulating film separated in a vertical direction on the first conductive film located on a sidewall of the island-like semiconductor layer;
separating the first conductive film using the sidewall spacers as a mask;
introducing an impurity in self-alignment with respect to the separated first conductive films; and
forming an interlayer insulating film and a second conductive film on the first conductive films.

**[0042]** The present invention further provides a process for producing a semiconductor memory having at least one memory cell constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;
forming a charge storage layer of a laminated insulating film and a first conductive film over a surface of the island-like semiconductor layer;
forming sidewall spacers of an insulating film separated in a vertical direction on the first conductive film located on a sidewall of the island-like semiconductor layer;
separating the first conductive film using the sidewall spacers as a mask; and
introducing an impurity in self-alignment with respect to the separated first conductive films.

**[0043]** The present invention also provides a process for producing a semiconductor memory having at least one memory cell constituted of an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;
introducing an impurity partially in the island-like semiconductor layer;
forming an insulating film and a first conductive film over a surface of the island-like semiconductor layer;
forming sidewall spacers of an insulating film separated in a vertical direction on the first conductive film located on a sidewall of the island-like semiconductor layer; and
separating the first conductive film using the sidewall spacers as a mask.

**[0044]** These and other objects of the present application will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0045]**

Fig. 1 is a plan view illustrating a memory cell array of an EEPROM having floating gates as charge storage layers in accordance with the present invention;

Fig. 2 to Fig. 64 are plan views illustrating other memory cell arrays of EEPROMs having floating gates as charge storage layers in accordance with the present invention;

Fig. 65 is a plan view illustrating a memory cell array of a MONOS structure having laminated insulating films as charge storage layers in accordance with the present invention;

Fig. 66 is a plan view illustrating a memory cell array of a DRAM structure having MIS capacitors as charge storage layers in accordance with the present invention;

Fig. 67 is a plan view illustrating a memory cell array of a SRAM structure having MIS transistors as charge storage layers in accordance with the present invention;

Fig. 68 to Fig. 72 are plan views illustrating other memory cell arrays of EEPROMs having floating gates as charge storage layers in accordance with the present invention;

Fig. 73 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 74 is a sectional view of another semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 75 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 76 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 77 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 78 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 79 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 80 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 81 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 82 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 83 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 84 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 85 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 86 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 87 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 88 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 89 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 90 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 91 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 92 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 93 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 94 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 95 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 96 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 97 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 98 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 99 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 100 is a sectional view of a semiconductor memory having floating gates as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 101 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers in accordance with the present invention, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 102 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers in accordance with the present invention, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 103 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 104 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 105 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 106 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 107 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 108 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 109 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 110 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 111 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 112 is a sectional view of a semiconductor memory having laminated insulating films as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 113 is a sectional view of a semiconductor memory having MIS capacitors as charge storage layers in accordance with the present invention, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 114 is a sectional view of a semiconductor memory having MIS capacitors as charge storage layers in accordance with the present invention, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 115 is a sectional view of a semiconductor memory having MIS capacitors as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 116 is a sectional view of a semiconductor memory having MIS capacitors as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 117 is a sectional view of a semiconductor memory having MIS capacitors as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 118 is a sectional view of a semiconductor memory having MIS capacitors as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 119 is a sectional view of a semiconductor memory having MIS transistors as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 120 is a sectional view of a semiconductor memory having MIS transistors as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 121 is a sectional view of a semiconductor memory having MIS transistors as charge storage layers, corresponding to a sectional view as taken on line A-A' in Fig. 1;

Fig. 122 is a sectional view of a semiconductor memory having MIS transistors as charge storage layers, corresponding to a sectional view as taken on line B-B' in Fig. 1;

Fig. 123 to Fig. 178 are equivalent circuit diagrams of semiconductor memories in accordance with the present invention;

Fig. 179 to Fig. 198 show examples of timing charts at reading data from semiconductor memories in accordance with the present invention;

Fig. 199 to Fig. 235 show examples of timing charts at writing data in semiconductor memories in ac-

cordance with the present invention;
Fig. 236 to Fig. 278 show examples of timing charts at erasing data from semiconductor memories in accordance with the present invention;
Fig. 279 to 298 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 1 for producing a semiconductor memory in accordance with the present invention;
Fig. 299 to Fig. 317 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 1 for producing a semiconductor memory in accordance with the present invention;
Fig. 318 to Fig. 325 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 2 for producing a semiconductor memory in accordance with the present invention;
Fig. 326 to Fig. 333 are sectional views (taken on line-B-B' in Fig. 1) illustrating production steps of Production Example 2 for producing a semiconductor memory in accordance with the present invention;
Fig. 334 to Fig. 336 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 2 for producing a semiconductor memory in accordance with the present invention;
Fig. 337 to Fig. 339 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 2 for producing a semiconductor memory in accordance with the present invention;
Fig. 340 to Fig. 344 are sectional views (taken on line A-A' in Fig. 66) illustrating production steps of Production Example 3 for producing a semiconductor memory in accordance with the present invention;
Fig. 345 to Fig. 349 are sectional views (taken on line B-B' in Fig. 66) illustrating production steps of Production Example 3 for producing a semiconductor memory in accordance with the present invention;
Fig. 350 to Fig. 369 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 4 for producing a semiconductor memory in accordance with the present invention;
Fig. 370 to Fig. 389 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 4 for producing a semiconductor memory in accordance with the present invention;
Fig. 390 to Fig. 394 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 4 for producing a semiconductor memory in accordance with the present invention;
Fig. 395 to Fig. 399 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 4 for producing a semiconductor memory in accordance with the present invention;
Fig. 400 to Fig. 403 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 5 for producing a semiconductor memory in accordance with the present invention;
Fig. 404 to Fig. 412 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 6 for producing a semiconductor memory in accordance with the present invention;
Fig. 413 to Fig.421 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 6 for producing a semiconductor memory in accordance with the present invention;
Fig. 422 to Fig. 439 are sectional views (taken on line A-A' in Fig. 50) illustrating production steps of Production Example 7 for producing a semiconductor memory in accordance with the present invention;
Fig. 440 to Fig. 457 are sectional views (taken on line B-B' in Fig. 50) illustrating production steps of Production Example 7 for producing a semiconductor memory in accordance with the present invention;
Fig. 458 to Fig. 462 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 8 for producing a semiconductor memory in accordance with the present invention;
Fig. 463 to Fig. 467 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 8 for producing a semiconductor memory in accordance with the present invention;
Fig. 468 to Fig. 472 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 9 for producing a semiconductor memory in accordance with the present invention;
Fig. 473 to Fig. 477 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 9 for producing a semiconductor memory in accordance with the present invention;
Fig. 478 to Fig. 483 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 10 for producing a semiconductor memory in accordance with the present invention;
Fig. 484 to Fig. 489 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 10 for producing a semicon-

ductor memory in accordance with the present invention;

Fig. 490 to Fig. 495 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 11 for producing a semiconductor memory in accordance with the present invention;

Fig. 496 to Fig.501 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 11 for producing a semiconductor memory in accordance with the present invention;

Fig. 502 is a sectional view (taken on line A-A' in Fig. 1) illustrating a production step of Production Example 12 for producing a semiconductor memory in accordance with the present invention;

Fig. 503 is a sectional view (taken on line B-B' in Fig. 1) illustrating a production step of Production Example 12 for producing a semiconductor memory in accordance with the present invention;

Fig. 504 is a sectional view (taken on line A-A' in Fig. 1) illustrating a production step of Production Example 13 for producing a semiconductor memory in accordance with the present invention;

Fig. 505 is a sectional view (taken on line B-B' in Fig. 1) illustrating a production step of Production Example 13 for producing a semiconductor memory in accordance with the present invention;

Fig. 506 is a sectional view (taken on line A-A' in Fig. 1) illustrating a production step of Production Example 14 for producing a semiconductor memory in accordance with the present invention;

Fig. 507 is a sectional view (taken on line B-B' in Fig. 1) illustrating a production step of Production Example 14 for producing a semiconductor memory in accordance with the present invention;

Fig. 508 is a sectional view (taken on line A-A' in Fig. 1) illustrating a production step of Production Example 14 for producing a semiconductor memory in accordance with the present invention;

Fig. 509 is a sectional view (taken on line B-B' in Fig. 1) illustrating a production step of Production Example 14 for producing a semiconductor memory in accordance with the present invention;

Fig. 510 is a sectional view (taken on line A-A' in Fig. 1) illustrating a production step of Production Example 15 for producing a semiconductor memory in accordance with the present invention;

Fig. 511 is a sectional view (taken on line B-B' in Fig. 1) illustrating a production step of Production Example 15 for producing a semiconductor memory in accordance with the present invention;

Fig. 512 and Fig. 513 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 16 for producing a semiconductor memory in accordance with the present invention;

Fig. 514 and Fig. 515 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 16 for producing a semiconductor memory in accordance with the present invention;

Fig. 516 to Fig. 523 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 17 for producing a semiconductor memory in accordance with the present invention;

Fig. 524 to Fig. 531 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 17 for producing a semiconductor memory in accordance with the present invention;

Fig. 532 and Fig. 533 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 18 for producing a semiconductor memory in accordance with the present invention;

Fig. 534 and Fig. 535 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 18 for producing a semiconductor memory in accordance with the present invention;

Fig. 536 and Fig. 537 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 19 for producing a semiconductor memory in accordance with the present invention;

Fig. 538 and Fig. 539 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 19 for producing a semiconductor memory in accordance with the present invention;

Fig. 540 to Fig. 562 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 20 for producing a semiconductor memory in accordance with the present invention;

Fig. 563 to Fig. 585 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 20 for producing a semiconductor memory in accordance with the present invention;

Fig. 586 to Fig. 605 are sectional views (taken on line E-E' in Fig. 1) illustrating production steps of Production Example 21 for producing a semiconductor memory in accordance with the present invention;

Fig. 606 to Fig. 613 are sectional views (taken on line F-F' in Fig. 1) illustrating production steps of Production Example 21 for producing a semiconductor memory in accordance with the present invention;

Fig. 614 to Fig. 636 are sectional views (taken on line G-G' in Fig. 1) illustrating production steps of Production Example 21 for producing a semiconductor memory in accordance with the present in-

vention;
Fig. 637 to Fig. 647 are sectional views (taken on line E-E' in Fig. 1) illustrating production steps of Production Example 22 for producing a semiconductor memory in accordance with the present invention;
Fig. 648 to Fig. 658 are sectional views (taken on line F-F' in Fig. 1) illustrating production steps of Production Example 22 for producing a semiconductor memory in accordance with the present invention;
Fig. 659 to Fig. 669 are sectional views (taken on line G-G' in Fig. 1) illustrating production steps of Production Example 22 for producing a semiconductor memory in accordance with the present invention;
Fig. 670 is a sectional view (taken on line H-H' in Fig. 60) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 671 is a sectional view (taken on line I1-I1' in Fig. 60) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 672 is a sectional view (taken on line I2-I2' in Fig. 60) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 673 is a sectional view (taken on line I3-I3' in Fig. 60) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 674 is a sectional view (taken on line 14-14' in Fig. 60) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 675 is a sectional view (taken on line I5-I5' in Fig. 60) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 676 is a sectional view (taken on line H-H' in Fig. 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 677 is a sectional view (taken on line I1-I1' in Fig. 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 678 is a sectional view (taken on line I2-I2' in Fig. 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 679 is a sectional view (taken on line I3-I3' in Fig. 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 680 is a sectional view (taken on line I4-I4' in Fig. 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 681 is a sectional view (taken on line I5-I5' in Fig. 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 682 is a sectional view (taken on line H-H' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 683 is a sectional view (taken on line I1-I1' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 684 is a sectional view (taken on line I2-I2' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 685 is a sectional view (taken on line I3-I3' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 686 is a sectional view (taken on line I4-I4' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 687 is a sectional view (taken on line I5-I5' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 688 is a sectional view (taken on line H-H' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 689 is a sectional view (taken on line I1-I1' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 690 is a sectional view (taken on line I2-I2' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 691 is a sectional view (taken on line I3-I3' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 692 is a sectional view (taken on line I4-I4' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 693 is a sectional view (taken on line I5-I5' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 694 is a sectional view (taken on line H-H' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;

Fig. 695 is a sectional view (taken on line I1-I1' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 696 is a sectional view (taken on line I2-I2' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 697 is a sectional view (taken on line I3-I3' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 698 is a sectional view (taken on line I4-I4' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 699 is a sectional view (taken on line I5-I5' in Fig. 60 or 61) illustrating a production step of Production Example 23 for producing a semiconductor memory in accordance with the present invention;
Fig. 700 to Fig. 706 are sectional views (taken on line A-A' in Fig. 1) illustrating production steps of Production Example 24 for producing a semiconductor memory in accordance with the present invention;
Fig. 707 to Fig. 713 are sectional views (taken on line B-B' in Fig. 1) illustrating production steps of Production Example 24 for producing a semiconductor memory in accordance with the present invention;
Fig. 714 to Fig. 720 are sectional views (taken on line A-A' in Fig. 64) illustrating production steps of Production Example 25 for producing a semiconductor memory in accordance with the present invention;
Fig. 721 to Fig. 727 are sectional views (taken on line B-B' in Fig. 64) illustrating production steps of Production Example 25 for producing a semiconductor memory in accordance with the present invention;
Fig. 728 is a sectional view (taken on line H-H' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 729 is a sectional view (taken on line I1-I1' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 730 is a sectional view (taken on line I2-I2' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 731 is a sectional view (taken on line I3-I3' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 732 is a sectional view (taken on line I4-I4' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 733 is a sectional view (taken on line J1-J1' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 734 is a sectional view (taken on line J2-J2' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 735 is a sectional view (taken on line J3-J3' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 736 is a sectional view (taken on line J4-J4' in Fig. 70) illustrating a production step of Production Example 26 for producing a semiconductor memory in accordance with the present invention;
Fig. 737 is a sectional view (taken on line H-H' in Fig. 71) illustrating a production step of Production Example 27 for producing a semiconductor memory in accordance with the present invention;
Fig. 738 is a sectional view (taken on line I1-I1' in Fig. 71) illustrating a production step of Production Example 27 for producing a semiconductor memory in accordance with the present invention;
Fig. 739 is a sectional view (taken on line I2-I2' in Fig. 71) illustrating a production step of Production Example 27 for producing a semiconductor memory in accordance with the present invention;
Fig. 740 is a sectional view (taken on line I3-I3' in Fig. 71) illustrating a production step of Production Example 27 for producing a semiconductor memory in accordance with the present invention;
Fig. 741 is a sectional view (taken on line I4-I4' in Fig. 71) illustrating a production step of Production Example 27 for producing a semiconductor memory in accordance with the present invention;
Fig. 742 is a sectional view (taken on line H-H' in Fig. 72) illustrating a production step of Production Example 28 for producing a semiconductor memory in accordance with the present invention;
Fig. 743 is a sectional view (taken on line I1-I1' in Fig. 72) illustrating a production step of Production Example 28 for producing a semiconductor memory in accordance with the present invention;
Fig. 744 is a sectional view (taken on line I2-I2' in Fig. 72) illustrating a production step of Production Example 28 for producing a semiconductor memory in accordance with the present invention;
Fig. 745 is a sectional view (taken on line I3-I3' in Fig. 72) illustrating a production step of Production Example 28 for producing a semiconductor memory in accordance with the present invention;
Fig. 746 is a sectional view (taken on line I4-I4' in Fig. 72) illustrating a production step of Production Example 28 for producing a semiconductor memory in accordance with the present invention;

Fig. 747 is a sectional view (taken on line I5-I5' in Fig. 72) illustrating a production step of Production Example 28 for producing a semiconductor memory in accordance with the present invention;

Fig. 748 is a sectional view (taken on line H-H' in Fig. 74) illustrating a production step of Production Example 29 for producing a semiconductor memory in accordance with the present invention;

Fig. 749 to Fig. 753 are sectional views (shifted in parallel in a H-H' direction within a lead-out portion of a wiring layer in a sectional view taken on line I-I' in Fig. 68) illustrating production steps of Production Example 29 for producing a semiconductor memory in accordance with the present invention;

Fig. 754 is a sectional view (taken on line A-A' in Fig. 1) illustrating a production step of Production Example 30 for producing a semiconductor memory in accordance with the present invention;

Fig. 755 is a sectional view (taken on line B-B' in Fig. 1) illustrating a production step of Production Example 30 for producing a semiconductor memory in accordance with the present invention;

Fig. 756 to Fig. 764 are sectional views (taken on line A-A' in Fig. 66) illustrating production steps of Production Example 31 for producing a semiconductor memory in accordance with the present invention;

Fig. 765 to Fig. 773 are sectional views (taken on line B-B' in Fig. 66) illustrating production steps of Production Example 31 for producing a semiconductor memory in accordance with the present invention;

Fig. 774 is a sectional view (taken on line A-A' in Fig. 66) illustrating a production step of Production Example 31 for producing a semiconductor memory in accordance with the present invention;

Fig. 775 is a sectional view (taken on line B-B' in Fig. 66) illustrating a production step of Production Example 31 for producing a semiconductor memory in accordance with the present invention;

Fig. 776 is a sectional view (taken on line H-H' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 777 is a sectional view (taken on line I1-I1' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 778 is a sectional view (taken on line I2-I2' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 779 is a sectional view (taken on line I3-I3' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 780 is a sectional view (taken on line I4-I4' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 781 is a sectional view (taken on line I5-I5' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 782 is a sectional view (taken on line H-H' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 783 is a sectional view (taken on line I1-I1' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 784 is a sectional view (taken on line I2-I2' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 785 is a sectional view (taken on line I3-I3' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 786 is a sectional view (taken on line I4-I4' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 787 is a sectional view (taken on line I5-I5' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 788 is a sectional view (taken on line H-H' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 789 is a sectional view (taken on line I1-I1' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 790 is a sectional view (taken on line I2-I2' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 791 is a sectional view (taken on line I3-I3' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 792 is a sectional view (taken on line I4-I4' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 793 is a sectional view (taken on line I5-I5' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 794 is a sectional view (taken on line H-H' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 795 is a sectional view (taken on line I1-I1' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 796 is a sectional view (taken on line I2-I2' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 797 is a sectional view (taken on line I3-I3' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 798 is a sectional view (taken on line I4-I4' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 799 is a sectional view (taken on line I5-I5' in Fig. 62) illustrating a production step of Production Example 32 for producing a semiconductor memory in accordance with the present invention;

Fig. 800 is a plan view illustrating a prior-art EEPROM;

Fig. 801 shows sectional views taken on line A-A' and line B-B' in Fig. 800;

Fig. 802 to Fig. 805 are sectional views illustrating production steps for producing a prior-art EEPROM;

Fig. 806 shows a plan view illustrating a prior-art EEPROM and a corresponding equivalent circuit;

Fig. 807 is a sectional view of a conventional memory cell of an NMOS structure;

Fig. 808 is a sectional view of another prior-art memory cell of the NMOS structure; and

Fig. 809 is a sectional view of a semiconductor device having a plurality of memory cells on one pillar-form silicon layer.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0046]** The semiconductor memory of the present invention mainly has a first conductivity type semiconductor substrate and one or more memory cells. The memory cell is constituted of an island-like semiconductor layer, at least one charge storage layer and at least one control gate (a third electrode). The charge storage layer and the control gate is formed around a sidewall of the island-like semiconductor layer. At least one of said one or more memory cells is electrically insulated from the semiconductor substrate.

**[0047]** That "at least one of said one or more memory cells is electrically insulated from the semiconductor substrate" means that the island-like semiconductor layer is electrically insulated from the semiconductor substrate. If two or more memory cells are formed in one island-like semiconductor layer, memory cells are electrically insulated and thereby a memory cell/memory cells above an insulating site is/are electrically insulated from the semiconductor substrate. If a selection gate (memory gate) is formed below the memory cell(s), a selection transistor composed of the selection gate is electrically insulated from the semiconductor substrate or the selection transistor is electrically insulated from a memory cell and thereby a memory cell/memory cells above an insulating site is/are electrically insulated from the semiconductor substrate. It is preferably in particular that the selection transistor is formed between the semiconductor substrate and the island-like semiconductor layer or below the memory cell(s) and the selection transistor is electrically insulated from the semiconductor substrate.

**[0048]** Electric insulation may be made, for example, by forming a second conductivity type impurity diffusion layer over a region to be insulated, by forming the second conductivity type impurity diffusion layer in part of the region to be insulated and utilizing a depletion layer at a junction of the second conductivity type impurity diffusion layer, or by providing a distance not allowing electric conduction and achieving electric insulation as a result. The semiconductor substrate may be electrically insulated from the memory cell(s) or the selection transistor by an insulating film of $SiO_2$ or the like. In the case where a plurality of memory cells are formed in one island-like semiconductor layer and selection transistors are optionally formed above or below the memory cells, the electric insulation may be formed between optional memory cells and/or a selection transistor and a memory cell.

**[0049]** The charge storage layer and the control gate may be formed all around the sidewall of the island-like semiconductor layer or on a part of the sidewall.

**[0050]** Only one memory cell or two or more memory cells may be formed on one island-like semiconductor layer. If three or more memory cells are formed, a selection gate is preferably formed below or above the memory cells to form a selection transistor together with the island-like semiconductor layer.

**[0051]** Hereinafter, are explained constructions in which a plurality of, for example, two memory cells are arranged in series on one island-like semiconductor layer, island-like semiconductor layers are arranged in matrix and selection transistors are disposed below and above the memory cells. A gate electrode of the selection transistor below the memory cells is represented as a second electrode and a gate electrode of the selection transistor above the memory cells is represented as a fifth electrode. A tunnel insulating film is represented as a third insulating film, a sidewall spacer is represented as a fourth insulating film, and a gate insulating film which is a part of the selection transistor is represented as a thirteenth insulating film.

**[0052]** In the above-mentioned semiconductor memory, an impurity diffusion layer for reading the state of a charge stored in the memory cells is formed as a source or drain (first wiring) of the memory cells in the island-like semiconductor layer. This impurity diffusion layer

electrically insulates the island-like semiconductor layer from the semiconductor substrate. Control gates formed in a plurality of island-like semiconductor layers are arranged continuously in one direction to form a control gate line (third wiring). Another impurity diffusion layer is formed as a source or drain of the memory cells in the island-like semiconductor layer and a plurality of such impurity diffusion layers in a direction crossing the control gate line are electrically connected to form a bit line (fourth wiring).

**[0053]** Although the control gate line and the bit line orthogonal to the control gate may be in any three-dimensional directions, are explained hereinafter constructions in which the lines are formed in directions horizontal to the semiconductor substrate.

Embodiments of memory cell arrays as shown in plan views

**[0054]** The memory cell array in the semiconductor memory of the present invention is described with reference to plan views shown in Fig. 1 to Fig. 72. Figs. 1 to 64 and Figs. 68 to 72 illustrate examples of EEPROM memory cell arrays having floating gates as charge storage layers. Fig. 65 illustrates a memory cell array of MONOS structure having laminated insulating films as charge storage layers, Fig. 66 illustrates a memory cell array of DRAM structure having MIS capacitors as charge storage layers, and Fig. 67 illustrates a memory cell array of SRAM structure having MIS transistors as charge storage layers. These figures also illustrate layouts of second or fifth wiring as gate electrodes for selecting memory cells (referred to as "selection gates" hereinafter), third wiring as control gates, fourth wiring as bit lines and first wiring as source lines. Selection gate transistors are not shown for avoiding complexity.

**[0055]** First, explanation is given of the EEPROM memory cell arrays having floating gates as charge storage layers.

**[0056]** In Fig. 1, island-like semiconductor layers in a columnar form for constituting memory cells are arranged to be located at intersections where a group of parallel lines and another group of parallel lines cross at right angles. First, second, third and fourth wiring layers for selecting and controlling the memory cells are disposed in parallel to the surface of the substrate.

**[0057]** By changing intervals between island-like semiconductor layers between an A-A' direction which crosses fourth wiring layers 840 and a B-B' direction which is parallel to the fourth wiring layers 840, second conductive films which act as the control gates of the memory cells are formed continuously in one direction, in the A-A' direction in Fig. 1, to be the third wiring layers. Likewise, second conductive films which act as the gates of the selection gate transistors are formed continuously in one direction to be the second wiring layers.

**[0058]** A terminal for electrically connecting with the first wiring layer disposed on a substrate side of island-like semiconductor layers is provided, for example, at an A' side end of a row of memory cells connected in the A-A' direction in Fig. 1, and terminals for electrically connecting with the second and third wiring layers are provided at an A side end of the row of memory cells connected in the A-A' direction in Fig. 1. The fourth wiring layers 840 disposed on a side of the island-like semiconductor layers opposite to the substrate are electrically connected to the island-like semiconductor layers in the columnar form for constituting memory cells. In Fig. 1, the fourth wiring layers 840 are formed in the direction crossing the second and third wiring layers.

**[0059]** The terminals for electrically connecting with the first wiring layers are formed of island-like semiconductor layers, and the terminals for electrically connecting with the second and third wiring layers are formed of second conductive films covering the island-like semiconductor layers, respectively. The terminals for electrically connecting with the first, second and third wiring layers are connected to first contacts 910, second contacts 921 and 924 and third contacts 932, respectively. In Fig. 1, the first wiring layers 810 are lead out onto the top of the semiconductor memory via the first contacts.

**[0060]** The island-like semiconductor layers in the columnar form for constituting the memory cells may be not only in the form of a column but also in the form of a prism, a polygonalar prism or the like. In the case where they are patterned in columns, it is possible to avoid occurrence of local field concentration on the surface of active regions and have an easy electrical control.

**[0061]** The arrangement of the island-like semiconductor layers in the columnar form is not particularly limited to that shown in Fig. 1 but may be any arrangement so long as the above-mentioned positional relationship and electric connection between the wiring layers are realized.

**[0062]** The island-like semiconductor layers connected to the first contacts 910 are all located at the A' side ends of the memory cells connected in the A-A' direction in Fig. 1. However, they may be located entirely or partially located on the A side ends or may be located at any of the island-like semiconductor layers constituting the memory cells connected in the A-A' direction. The island-like semiconductor layers covered with the second conductive films connected to the second contacts 921 and 924 and the third contacts 932 may be located at the ends where the first contacts 910 are not disposed, may be located adjacently to the island-like semiconductor layers connected to the first contacts 910 at the ends where the first contacts 910 are disposed, and may be located at any of the island-like semiconductor layers constituting the memory cells connected in the A-A' direction. The second contacts 921 and 924 and the third contacts 932 may be located at different places. The width and shape of the first wiring layers 810 and the fourth wiring layers 840 are not particularly limited so long as a desired wiring can be obtained.

**[0063]** In the case where the first wiring layers, which are disposed on the substrate side of the island-like semiconductor layers, are formed in self-alignment with the second and third wiring layers formed of the second conductive films, the island-like semiconductor layers which act as the terminals for electrically connecting with the first wiring layers are electrically insulated from the second and third wiring layers but contact the second and third wiring layers with intervention of insulating films. In Fig. 1, for example, first conductive films are formed partially on the sidewalls of the island-like semiconductor layers connected to the first contacts 910 with intervention of insulating films. The first conductive films are located to face the island-like semiconductor layers for constituting the memory cells. The second conductive films are formed on the first conductive films with intervention of insulating films. The second conductive films are connected to the second and third wiring layers formed continuously in the A-A' direction. At this time, the shape of the first and the second conductive films is not particularly limited.

**[0064]** The first conductive films on the sidewalls of the island-like semiconductor layers which act as the terminals for electrically connecting with the first wiring layers may be removed by setting the distance from said island-like semiconductor layers to the first conductive films on the island-like semiconductor layers for constituting the memory cells, for example, to be two or less times larger than the thickness of the second conductive films. In Fig. 1, the second and third contacts are formed on the second wiring layers 821 and 824 and the third wiring layers 832 which are formed to cover the top of the island-like semiconductor layers. However, the shape of the second and third wiring layers is not particularly limited so long as their connection is realized. Fig. 1 also shows lines for sectional views to be used for explaining examples of production processes, i.e., A-A' line, B-B' line, C-C' line, D-D' line, E-E' line and F-F' line.

**[0065]** In Fig. 2, in contrast to Fig. 1, the fourth wiring layers 840 are so arranged that adjacent island-like semiconductor layers in the B-B' direction are not connected to the same fourth wiring layer. In this case, two contacts adjacent in the B-B' direction may be connected, for example, by metal wiring. More particularly, adjacent contacts 924 are connected by the second wiring layer 824, and likewise, adjacent contacts 921, 932 and 933 are connected with the second wiring layer 821, the third wiring layer 832 and the third wiring layer 833, respectively. The contacts 910 may also be connected in the same manner. Alternatively, contacts may be formed to connect, for example, adjacent second conductive films together instead of connecting contacts by wiring layers.

**[0066]** In Fig. 3, in contrast to Fig. 1, the connection relationship between the island-like semiconductor layers 110 and the wiring layers is shown over an extended range so that it is shown that M × N island-like semiconductor layers 110 (M and N are positive integers) are disposed. Fig. 3 shows width WB of the first wiring layers 810-1 to 810-N, width WA of the fourth wiring layer 840-1 to 840-N, the narrowest one SB1 of the intervals between the first wiring layers and the narrowest one SA1 of the intervals between the fourth wiring layers.

**[0067]** Fig. 3 shows a distance SC1 between 921-1 and 921-2 as an interval between second contacts.

**[0068]** Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583.

**[0069]** An equivalent circuit diagram of Fig. 3 is shown in Fig. 160.

**[0070]** In Fig. 4, in contrast to Fig. 3, adjacent island-like semiconductor layers 110 which act as lead-out portions of first wiring layers have different lengths in the A-A' direction. Island-like semiconductor layers 110 of two different lengths which act as lead-out portions of first wiring layers are alternatively disposed at the A' side end of the memory cell array. Thereby, the narrowest interval SB1 between the first wiring layers is ensured to increase.

**[0071]** The above-mentioned disposition may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end. So long as the above-mentioned disposition is realized, any first wiring layer may be optionally connected to either one of the island-like semiconductor layers 110 of the two different lengths.

**[0072]** Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583.

**[0073]** An equivalent circuit diagram of Fig. 4 is shown in Fig. 160.

**[0074]** In Fig. 5, in contrast to Fig. 3, adjacent island-like semiconductor layers 110 which act as lead-out portions of first wiring layers have different lengths in the A-A' direction. Island-like semiconductor layers 110 of more than two different lengths which act as lead-out portions of first wiring layers are disposed in a mountain form as shown in Fig. 5 at the A' side end of the memory cell array. Thereby, the narrowest interval SB1 between the first wiring layers is ensured to increase. The above-mentioned disposition may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end. So long as the above-mentioned disposition is realized, any first wiring layer may be optionally connected to any one of the island-like semiconductor layers 110 of more than two different lengths.

**[0075]** Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583.

**[0076]** An equivalent circuit diagram of Fig. 5 is shown in Fig. 160.

**[0077]** In Fig. 10, in contrast to Fig. 5, the above-mentioned disposition is realized alternately at the A side end and at the A' side end. An equivalent circuit diagram of Fig. 10 is shown in Fig. 167.

**[0078]** In Fig. 37, in contrast to Fig. 10, island-like semiconductor layers not connected to the fourth wiring layers are provided as dummies and disposed as shown in Fig. 37, instead of changing the length of the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers. Thereby, the memory cell array of Fig. 37 has the same effect as that of Fig. 10.

**[0079]** In Fig. 6, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are disposed alternately at the A side end and at the A' side end of the memory cell array.

**[0080]** Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583.

**[0081]** In Fig. 15, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers are disposed alternately at the A side end and at the A' side end of the memory cell array.

**[0082]** In Fig. 7, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers and the island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers are disposed alternately at the A side end and at the A' side end of the memory cell array. The lead-out portions of the first wiring layers are connected to the lead-out portions of the second and third wiring layers.

**[0083]** In Fig. 8, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers and the island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers are disposed alternately at the A side end and at the A' side end of the memory cell array. The lead-out portions of the first wiring layers and the lead-out portions of the second and third wiring layers are connected respectively to both the ends of the rows of the memory cells continuous in the A-A' direction.

**[0084]** Equivalent circuit diagrams of Fig. 6, Fig. 15, Fig. 7 and Fig. 8 are shown in Fig. 161, Fig. 163, Fig. 162 and Fig. 164, respectively.

**[0085]** In the case where the lead-out portions of the first wiring layers are contacted to the lead-out portions of the second and third wiring layers, the lead-out portions of the second and third wiring layers may be disposed nearer to the memory cell array or the lead-out portions of the first wiring layers may be disposed nearer to the memory cell array.

**[0086]** In Fig. 30, in contrast to Fig. 3, lead-out portions of the fourth wiring layers 840-1 to 840-M are disposed alternately at a B-side end and at a B'-side end of the memory cell array. An equivalent circuit diagram of Fig. 30 is shown in Fig. 176.

**[0087]** In Fig. 36, in contrast to Fig. 7, island-like semiconductor layers 110 not connected to the fourth wiring layers are provided between adjacent lead-out portions of the first wiring layers and between adjacent lead-out portions of the second and third wiring layers.

**[0088]** In Fig. 9, in contrast to Fig. 3, island-like semiconductor layers 110 not connected to the first wiring layers are provided as dummies to ensure spaces for placing the first wiring layers. The island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers have two or more different shapes and are disposed at the A' side end of the memory cell array as shown in Fig. 9. Thereby the narrowest interval SB1 between the first wiring layers is ensured to increase. One or a plurality of dummies may be provided in a plurality of rows of memory cells. The distance between the dummy and its adjacent island-like semiconductor layer in the B-B' direction may be equal or unequal to the intervals between the island-like semiconductor layers in the B-B' direction in the memory cell array. This applies not only to Fig. 9 but also to Fig. 12, Fig. 13, Fig. 16, Fig. 24 and Fig. 25. An equivalent circuit diagram of Fig. 9 is shown in Fig. 165.

**[0089]** The above-mentioned arrangement may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end. So long as the above-mentioned arrangement is realized, any first wiring layers may be optionally connected to any one of the island-like semiconductor layers 110 of the two or more different shapes.

**[0090]** In Fig. 14, in contrast to Fig. 9, the island-like semiconductor layers 110 not connected to the first wiring layers are not provided, but the above-mentioned arrangement at the A' side end is realized alternatively at the A side end and at the A' side end. An equivalent circuit diagram of Fig. 14 is shown in Fig. 166. This case is more advantageous than the case of Fig. 9 since the island-like semiconductor layers as the dummy are not provided and the memory cells can be more highly integrated.

**[0091]** In Fig. 35, in contrast to Fig. 9, the lead-out portions of the second and third wiring layers are disposed midway along the rows of memory cells continuous in the A-A' direction. An equivalent circuit diagram of Fig. 35 is shown in Fig. 173.

**[0092]** In Fig. 11, in contrast to Fig. 3, the positions of the first contacts 910 disposed in adjacent island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are shifted to each other in the A-A' direction. Thereby the narrowest interval SB1 between the first wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 11 is shown in Fig. 160.

**[0093]** The above-mentioned arrangement may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end.

**[0094]** In Fig. 12, in contrast to Fig. 3, island-like semiconductor layers 110 not connected to the first, second and third wiring layers are provided as dummyies to ensure spaces for placing the first, second and third wiring layers. The Island-like semiconductor layers 110 on which the memory cell are disposed are extended in the B-B' direction as they approach the lead-out portions of the first, second and third wiring layers. Thereby the narrowest interval SB1 between the first wiring layers is ensured to increase. The lead-out portions of the first wiring layers are contacted with the lead-out portions of the second and third wiring layers. An equivalent circuit diagram of Fig. 12 is shown in Fig. 168.

**[0095]** In Fig. 13, in contrast to Fig. 12, the lead-out portions of the first wiring layers are not contacted with the lead-out portions of the second and third wiring layers. The lead-out portions of the first wiring layers are disposed at the A' side end of the memory cell array and the lead-out portions of the second and third wiring layers are disposed at the A side end of the memory cell array. An equivalent circuit diagram of Fig. 13 is shown in Fig. 169.

**[0096]** In Fig. 16, in contrast to Fig. 3, island-like semiconductor layers 110 which connected to the second and third wiring layers are provided as dummies to ensure spaces for placing the second and third wiring layers. The island-like semiconductor layers 110 which are lead-out portions of the second and third wiring layers have two or more different shapes and are disposed at the A side end of the memory cell array, as shown in Fig. 16. Thereby the intervals between the second or third contacts, e.g., SC2 between 921-1 and 921-2 and between 921-3 and 921-4, SC3 between 921-2 and 921-3 and SC4 between 921-4 and 921-6, are ensured to increase as compared with Fig. 3. An equivalent circuit diagram of Fig. 16 is shown in Fig. 170.

**[0097]** The above-mentioned arrangement may be realized at the A' side end of the memory cell arrays or alternately at the A side end and at the A' side end.

**[0098]** In Fig. 20, in contrast to Fig. 16, the island-like semiconductor layers 110 not connected to the second and third wiring layers are not provided, but the above-mentioned arrangement at the A side end is realized alternatively at the A side end and at the A' side end. An equivalent circuit diagram of Fig. 20 is shown in Fig. 171. This case is more advantageous than the case of Fig. 16 since the memory cells can be more highly integrated since the island-like semiconductor layers as the dummies are not provided.

**[0099]** In Fig. 17, in contrast to Fig. 3, the positions of the second and third contacts 921, 932, 933 and 924 disposed in adjacent island-like semiconductor layers 110 which are lead-out portions of the second and third wiring layers are shifted to each other in the A-A' direction. Thereby the intervals between the second or third contacts, e.g., SC2 between 921-1 and 921-2 and between 921-3 and 921-4, SC3 between 921-2 and 921-3 and SC4 between 921-4 and 921-6, are ensured to increase as compared with Fig. 3. Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583. An equivalent circuit diagram of Fig. 17 is shown in Fig. 160.

**[0100]** The above-mentioned arrangement may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end.

**[0101]** In Fig. 18, in contrast to Fig. 3, adjacent island-like semiconductor layers 110 which act as lead-out portions of second and third wiring layers have different lengths in the A-A' direction. Island-like semiconductor layers 110 of two different lengths which act as lead-out portions of the second and third wiring layers are disposed at the A side end of the memory cell array. Thereby, the intervals between the second or third contacts, e.g., SC2 between 921-1 and 921-2, are ensured to increase as compared with Fig. 3. Also, in this case, the smallest interval between the second or third contacts, e.g., SC5 between 921-3 and 924-4, can be ensured to be larger than any interval between the second or third contacts in Fig. 3. This is an advantage because the second and third wiring layers can be formed more easily. An equivalent circuit diagram of Fig. 18 is shown in Fig. 160.

**[0102]** The above-mentioned arrangement may be realized at the A' side end of the memory cell array or alternately at the A side end and at the A' side end.

**[0103]** In Fig. 39, in contrast to Fig. 18, the difference of the length of adjacent island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers is about a disposition interval of the memory cells continuous in the A-A' direction. Thereby, the intervals between the second or third contacts, e.g., SC2 between 921-1 and 921-2, are ensured to increase as compared with Fig. 3. Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583.

**[0104]** In Fig. 19, in contrast to Fig. 3, adjacent island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers have different lengths in the A-A' direction. Island-like semiconductor layers 110 of more than two different lengths which act as lead-out portions of the second and third layers are disposed in a mountain form as shown in Fig. 19 at the A side end of the memory cell array. Thereby, the intervals between the second or third contacts, e.g., SC2 between 921-1 and 921-2 and SC3 between 921-2 and 921-3, are ensured to increase as compared with Fig. 3. In this case, the narrowest intervals between the second and third contacts, e.g., SC6 between 921-5 and 924-6 and SC7 between 921-6 and 924-7, are also ensured to be larger than any interval between the second and third contacts in Fig. 3. This arrangement has an advantage because the second and third wiring layers

can be formed more easily. An equivalent circuit diagram of Fig. 19 is shown in Fig. 160.

**[0105]** The above-mentioned arrangement may be realized at the A' side end of the memory cell array or alternately at the A side end and at the A' side end. So long as the above-mentioned arrangement is realized, the second and third wiring layers may be optionally connected to either one of the island-like semiconductor layers 110 of the more than two different lengths which act as the lead-out portions of the second and third wiring layers.

**[0106]** In Fig. 40, in contrast to Fig. 19, the difference in the more than two lengths of the island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers is about a disposition interval of the memory cells continuous in the A-A' direction, for example, as shown in Fig. 40. Thereby, the intervals between the second or third contacts, e.g., SC2 between 921-1 and 921-2 and SC3 between 921-2 and 921-3, are ensured to increase as compared with Fig. 3. Sectional views of a lead-out portion including the contacts 921, 932, 933 and 924 are shown in Fig. 658 and Fig. 669, and sectional views of a lead-out portion including the contact 910 are shown in Fig. 560 and Fig. 583. An equivalent circuit diagram of Fig. 18 is shown in Fig. 160.

**[0107]** In Fig. 38, in contrast to Fig. 19, island-like semiconductor layers 110 not connected to the fourth wiring layers are provided and disposed as dummies as shown in Fig. 38 without changing lengths of adjacent island-like semiconductor layers 110 which act as lead-out portions of the second and third wiring layers in the A-A' direction. Thereby, the same effect as obtained in Fig. 19 is obtained.

**[0108]** In Fig. 21, in contrast to Fig. 3, all the first contacts 910 are connected by a single first wiring layer 810. An equivalent circuit diagram of Fig. 21 is shown in Fig. 172.

**[0109]** The island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers may be disposed at the A side end of the memory cell array.

**[0110]** In Fig. 22, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are connected to first wiring layers 810 instead of forming the first contacts 910 in the island-like semiconductor layers 110. An equivalent circuit diagram of Fig. 22 is shown in Fig. 160.

**[0111]** In Fig. 23, in contrast to Fig. 3, all the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are connected to a single first wiring layer 810 instead of forming the first contacts 910 in the island-like semiconductor layers 110. An equivalent circuit diagram of Fig. 23 is shown in Fig. 172.

**[0112]** The island-like semiconductor layers 110 which act as the lead-out portions of the first wiring layers may be disposed at the A side end of the memory cell array.

**[0113]** In Fig. 24, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are connected to first wiring layers 810 instead of forming the first contacts 910 in the island-like semiconductor layers 110. Island-like semiconductor layers 110 not connected to the first wiring layers are provided as dummies to ensure spaces for placing the first wiring layers. The intervals between the first wiring layers 810-1, 810-2··· are set to be larger than the intervals between the island-like semiconductor layers 110 which act as the lead-out portions of the first wiring layers in the B-B' direction so that the narrowest interval SB1 between the first wiring layers is insured to be larger. An equivalent circuit diagram of Fig. 24 is shown in Fig. 165. By thus setting the intervals between the first wiring layers to be larger than those between the island-like semiconductor layers 110 which act as the lead-out portions of the first wiring layers, this arrangement has advantages in that the patterning of the first wiring layers becomes easier and the contacts for leading out the first wiring layers can be formed with an increased patterning margin.

**[0114]** In Fig. 25, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are connected to first wiring layers 810 instead of forming the first contacts 910 in the island-like semiconductor layers 110. Island-like semiconductor layers 110 not connected to the first wiring layers are provided as dummies to ensure spaces for placing the first wiring layers. The first wiring layers are formed into two or more different hook shapes and disposed at the A' side end of the memory cell array as shown in Fig. 25 so that the narrowest interval SB1 between the first wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 25 is shown in Fig. 165.

**[0115]** The above-mentioned arrangement may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end. So long as the above-mentioned arrangement is realized, the first wiring layers of the two or more different hook shapes may be optionally connected to any of the island-like semiconductor layers 110 which act as the lead-out portion of the first wiring layers.

**[0116]** In Fig. 26, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are connected to first wiring layers 810 instead of forming the first contacts 910 in the island-like semiconductor layers 110. First wiring layer of two different lengths are alternately disposed at the A' side end of the memory cell array. Thereby, the narrowest interval SB1 between the first wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 26 is shown in Fig. 160.

**[0117]** The above-mentioned arrangement may be realized at the A side end of the memory cell array or alternately at the A side end and at the A'-side end. So long as the above-mentioned arrangement is realized, the first wiring layers of the two different lengths may be

optionally connected to any of the island-like semiconductor layers 110 which act as the lead-out portions of the first wiring layers.

**[0118]** In Fig. 27, in contrast to Fig. 3, the island-like semiconductor layers 110 which act as lead-out portions of the first wiring layers are connected to first wiring layers 810 instead of forming the first contacts 910 in the island-like semiconductor layers 110. First wiring layers 810 of more than two different lengths are disposed in a mountain form as shown in Fig. 27 at the A' side end of the memory cell array. Thereby, the narrowest interval SB1 between the first wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 27 is shown in Fig. 160.

**[0119]** The above-mentioned arrangement may be realized at the A side end of the memory cell array or alternately at the A side end and at the A' side end. So long as the above-mentioned arrangement is realized, the first wiring layers of more than two different lengths may be optionally connected to any of the island-like semiconductor layers 110 which act as the lead-out portions of the first wiring layers.

**[0120]** In Fig. 28, in contrast to Fig. 3, island-like semiconductor layers 110 not connected to the fourth wiring layers are provided as dummies to ensure spaces for placing the fourth wiring layers. The intervals between the fourth wiring layers are set larger than the intervals between the island semiconductors 110 in the A-A' direction. Thereby, the narrowest interval SA1 between the fourth wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 28 is shown in Fig. 174. More particularly, in the case where there exist N first wiring layers, one fourth wiring layer is connected to N island semiconductor layers 110 as shown in Fig. 28. A fourth wiring layer, for example, 840-6, which is the nearest to the dummy island semiconductor layer 110-5 is shifted to the dummy island layer 110-5 side as it can be connected with an island-like semiconductor layer 110 to which 840-6 is to be connected. The fourth wiring layers 840 from a fourth wiring layer 840-7 are disposed at larger intervals than the intervals between the island-like semiconductor layers in the A-A' direction, as shown in Fig. 28. Where a fourth wiring layer 840 cannot connect with an island-like semiconductor layer 110 any more, a dummy island-like semiconductor layer 110 is provided. Thus, by providing larger intervals between the fourth wiring layers 840 than those between the island-like semiconductor layers 110 in the A-A' direction, this arrangement has advantages in that pattering for wiring becomes easier and the contacts 980 for leading out the fourth wiring layers 840 can be formed with an increased patterning margin. One or a plurality of dummy island-like semiconductor layers may be provided in the memory cell array. The distance in the A-A' direction from the dummy to an island-like semiconductor layer adjacent to the dummy may be equal or unequal to the intervals in the A-A' direction between the island-like semiconductor layers 110 in the memory array. This can apply not only to Fig. 28 but also to Fig. 29. The top of the dummy island semiconductor 110 may be fixed to a certain potential, preferably to the same potential as that of the first wiring layer 810 or to ground.

**[0121]** In Fig. 29, in contrast to Fig. 3, island-like semiconductor layers 110 not connected to the fourth wiring layers are provided as dummies to ensure spaces for placing the fourth wiring layers. The fourth wiring layers are formed into two or more hook shapes and disposed at the B' side end of the memory cell array, as shown in Fig. 29. Thereby, the narrowest interval SA1 between the fourth wiring layer is ensured to increase. An equivalent circuit diagram of Fig. 29 is shown in Fig. 175.

**[0122]** The above-mentioned arrangement may be realized at the B side end of the memory cell array or alternately at the B side end and at the B' side end. So long as the above-mentioned arrangement is realized, the fourth wiring layers of two or more different shapes may be optionally located anywhere. The top of the dummy island semiconductor layers 110 may be fixed to a certain potential, preferably to the same potential as that of the first wiring layer 810 or to ground.

**[0123]** In Fig. 34, in contrast to Fig. 29, the island-like semiconductor layers 110 not connected to the fourth wiring layers are not provided, but the above-mentioned arrangement at the B' side end is realized alternatively at the B side end and at the B' side end. An equivalent circuit diagram- of Fig. 34 is shown in Fig. 178. This case is more advantageous than the case of Fig. 29 since the memory cells can be more highly integrated since the dummy island-like semiconductor layers are not provided.

**[0124]** In Fig. 31, in contrast to Fig. 3, adjacent fourth wiring layers have different lengths in the B-B' direction. Fourth wiring layers of two different lengths are alternately disposed at the B' side end of the memory cell array. Thereby, the narrowest interval SA1 between the fourth wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 31 is shown in Fig. 160.

**[0125]** The above-mentioned arrangement may be realized at the B side end of the memory cell array or alternately at the B side end and at the B' side end. So long as the

**[0126]** above-mentioned arrangement is realized, the fourth wiring layers of two different lengths may be optionally located anywhere.

**[0127]** In Fig. 32, in contrast to Fig. 3, adjacent fourth wiring layers have different lengths in the B-B' direction. The fourth wiring layers have more than two different lengths and are disposed in a mountain form as shown in Fig. 32 at the B' side end of the memory cell array. Thereby, the narrowest interval SA1 between the fourth wiring layers is ensured to increase. An equivalent circuit diagram of Fig. 32 is shown in Fig. 160.

**[0128]** The above-mentioned arrangement may be realized at the B side end of the memory cell array or alternately at the B side end and at the B' side end. So long as the above-mentioned arrangement is realized,

Fig. 789

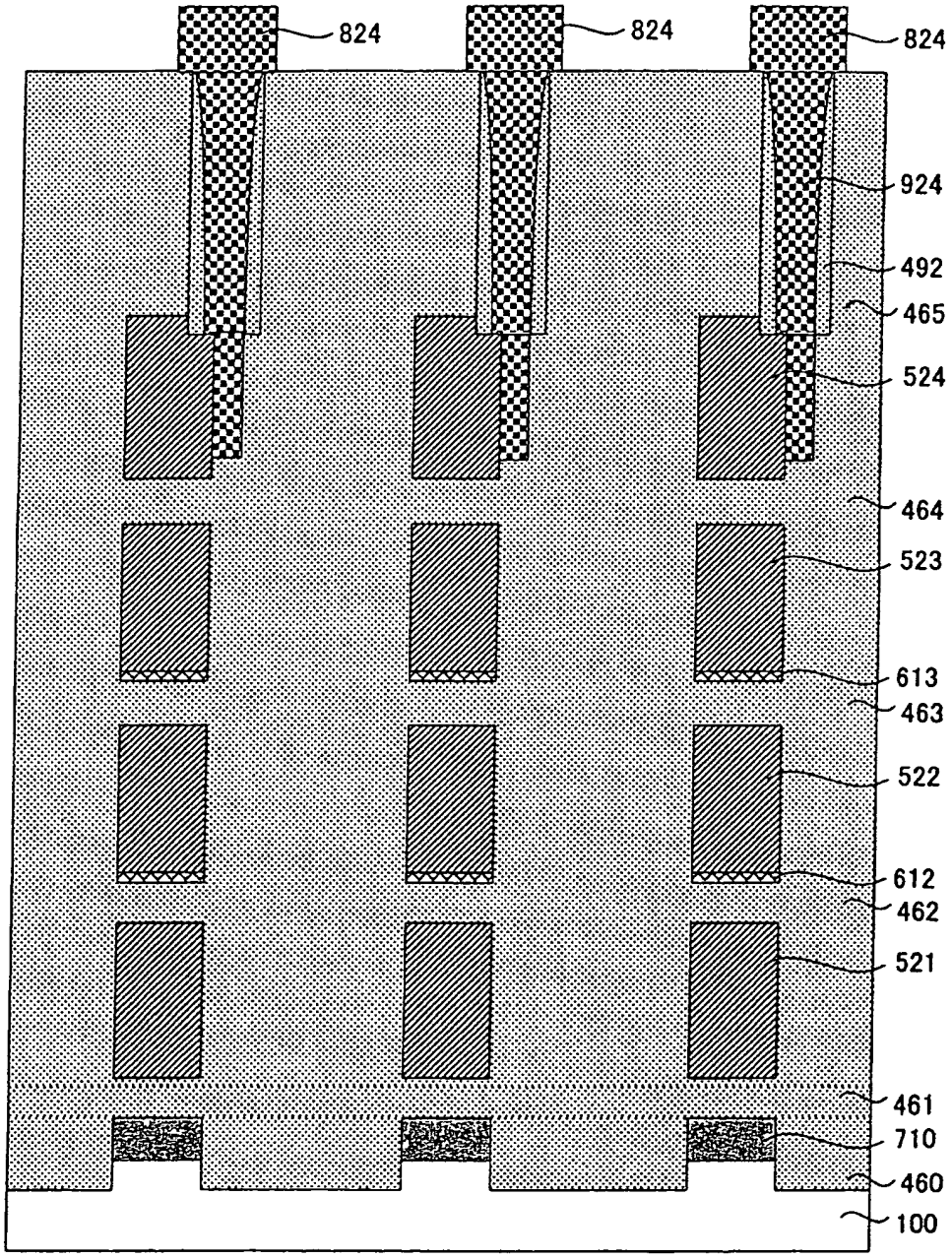
824
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Fig. 790

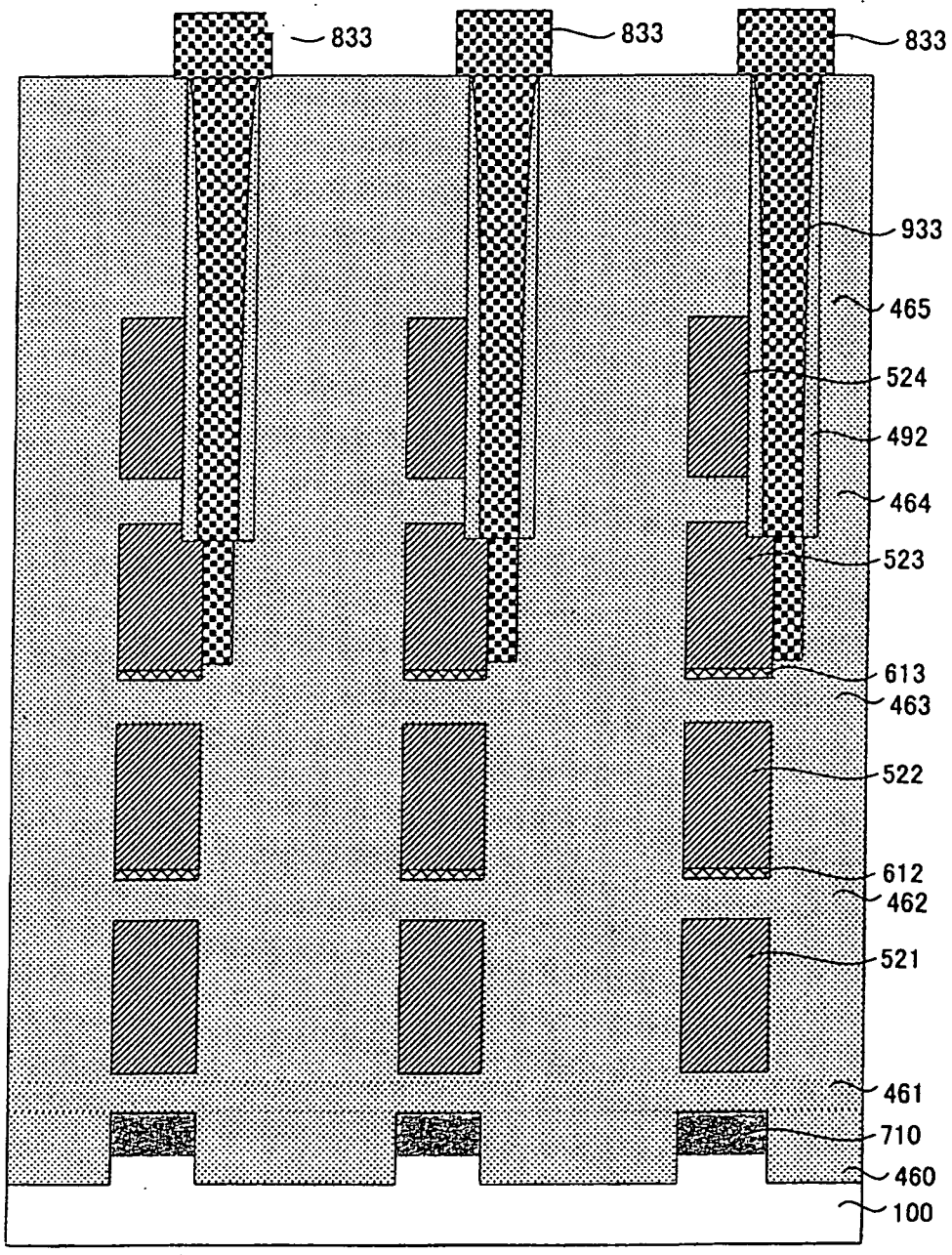
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Fig. 791

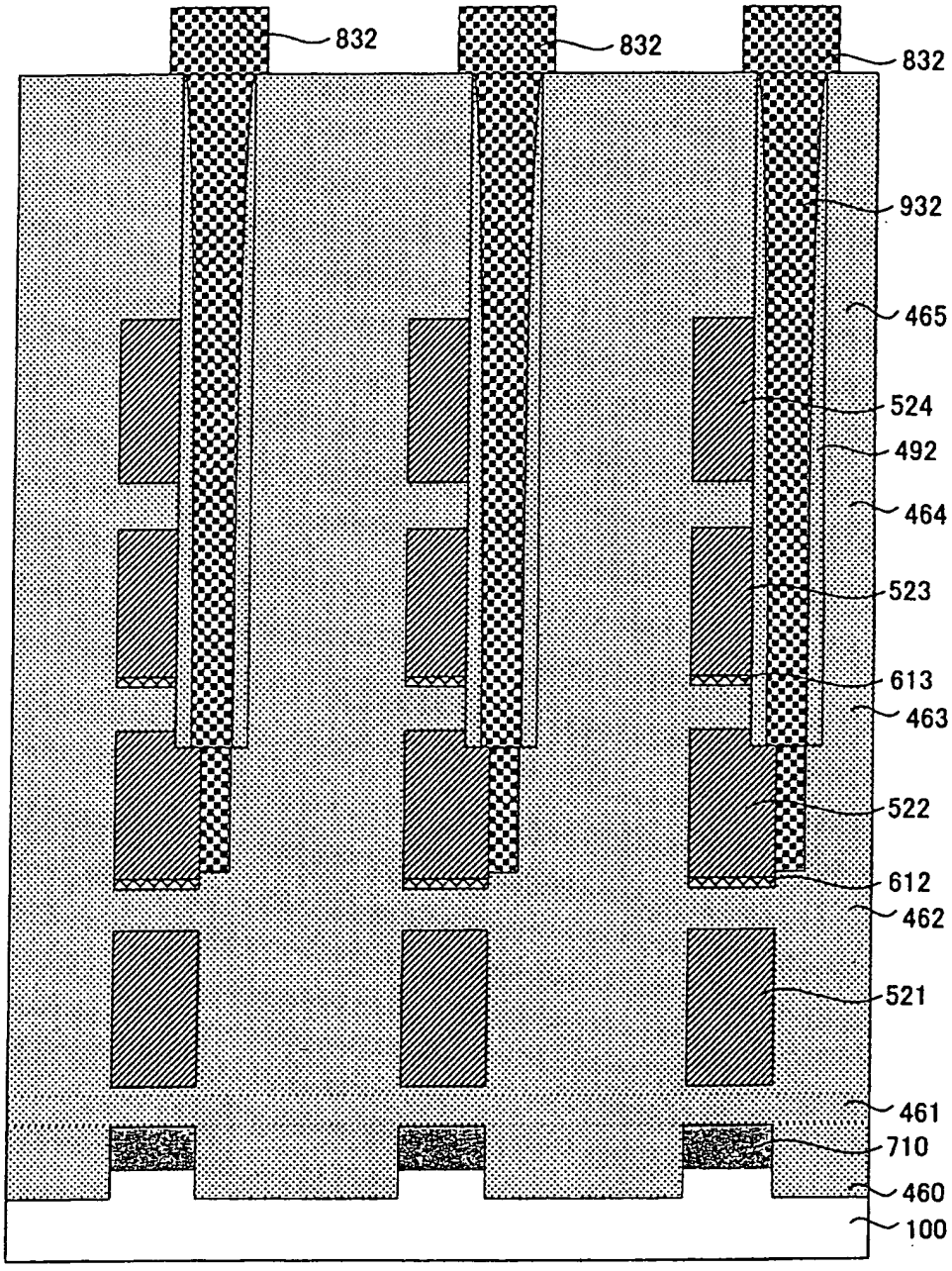
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Fig. 792

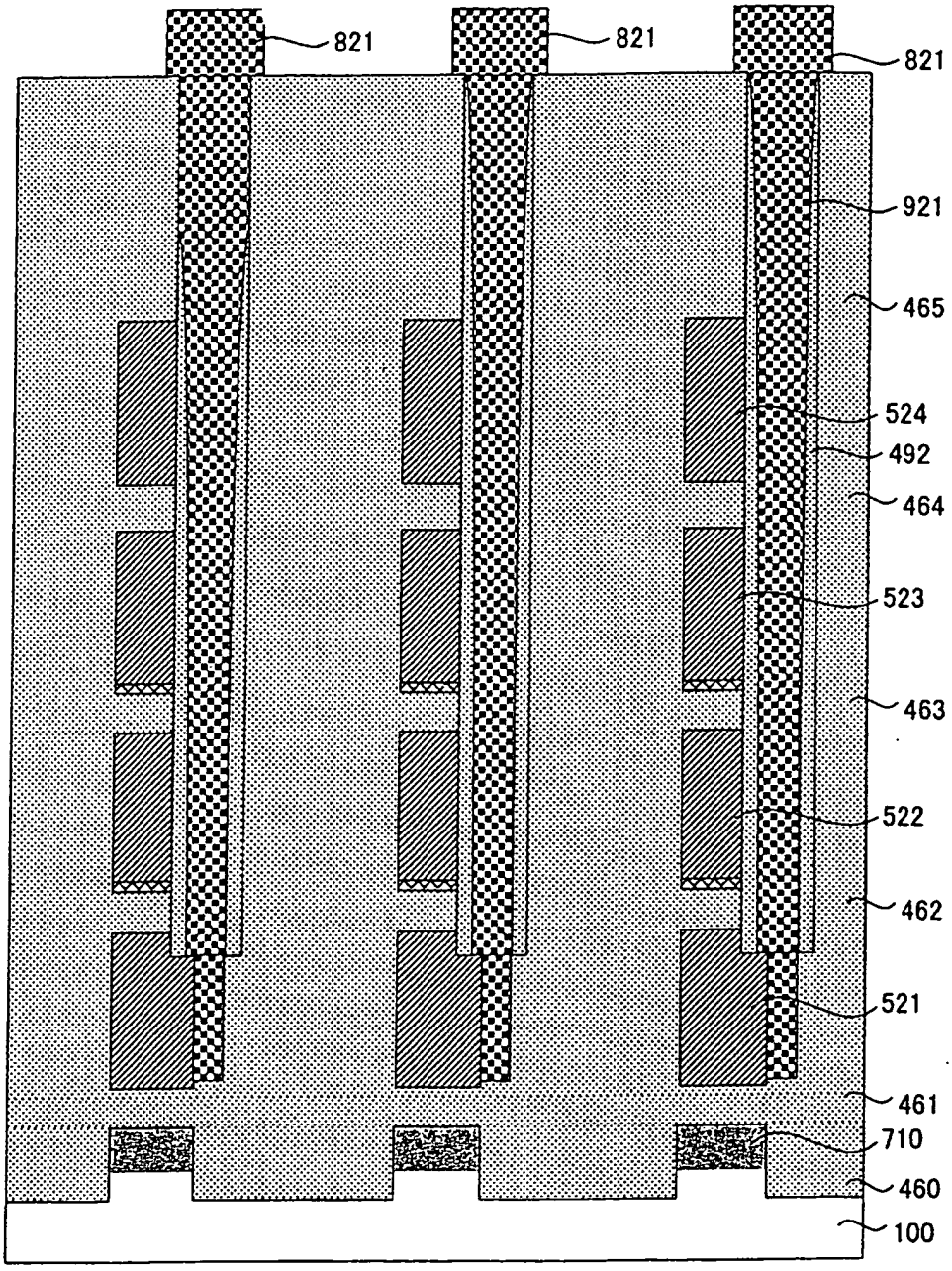
821
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Fig. 793

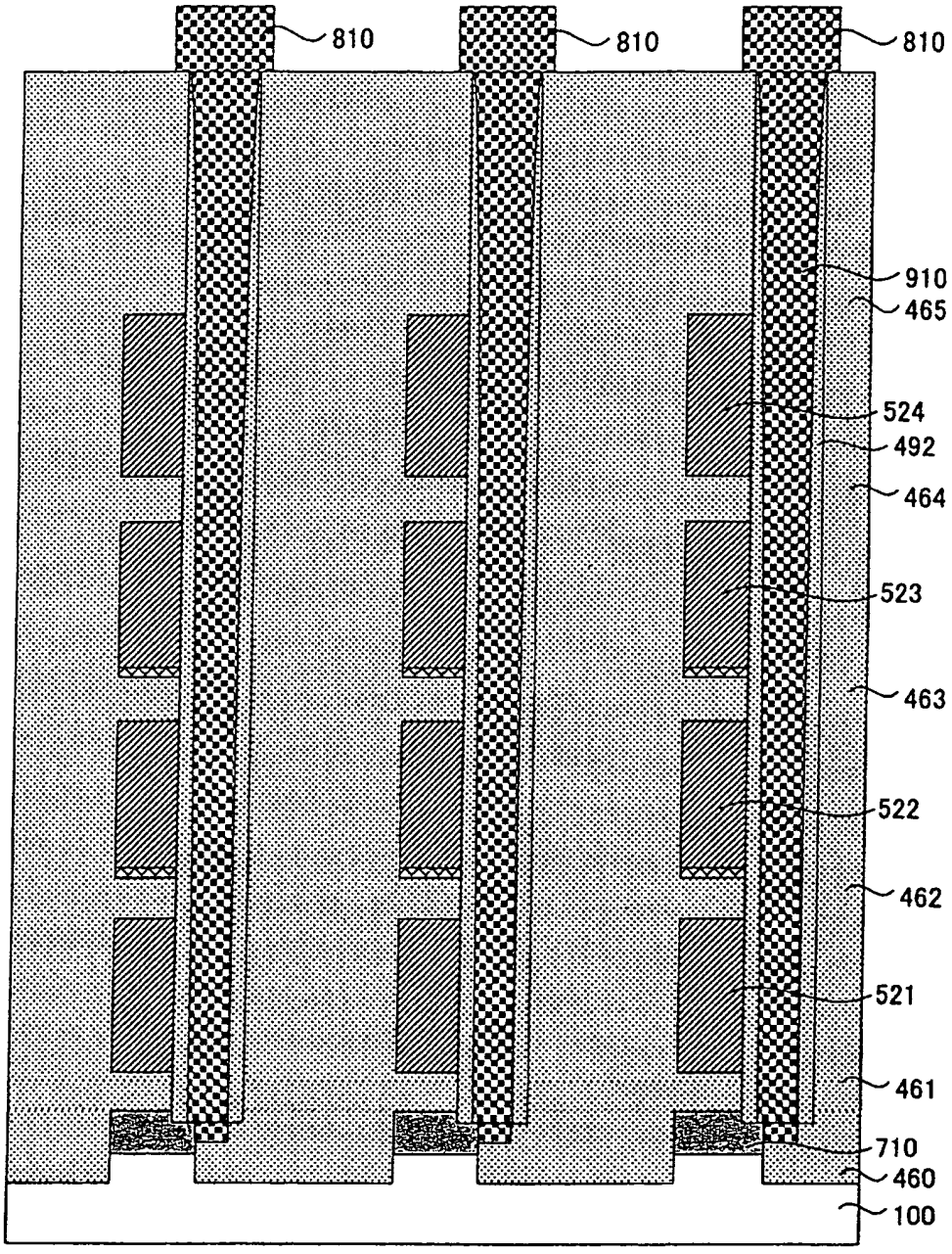
810
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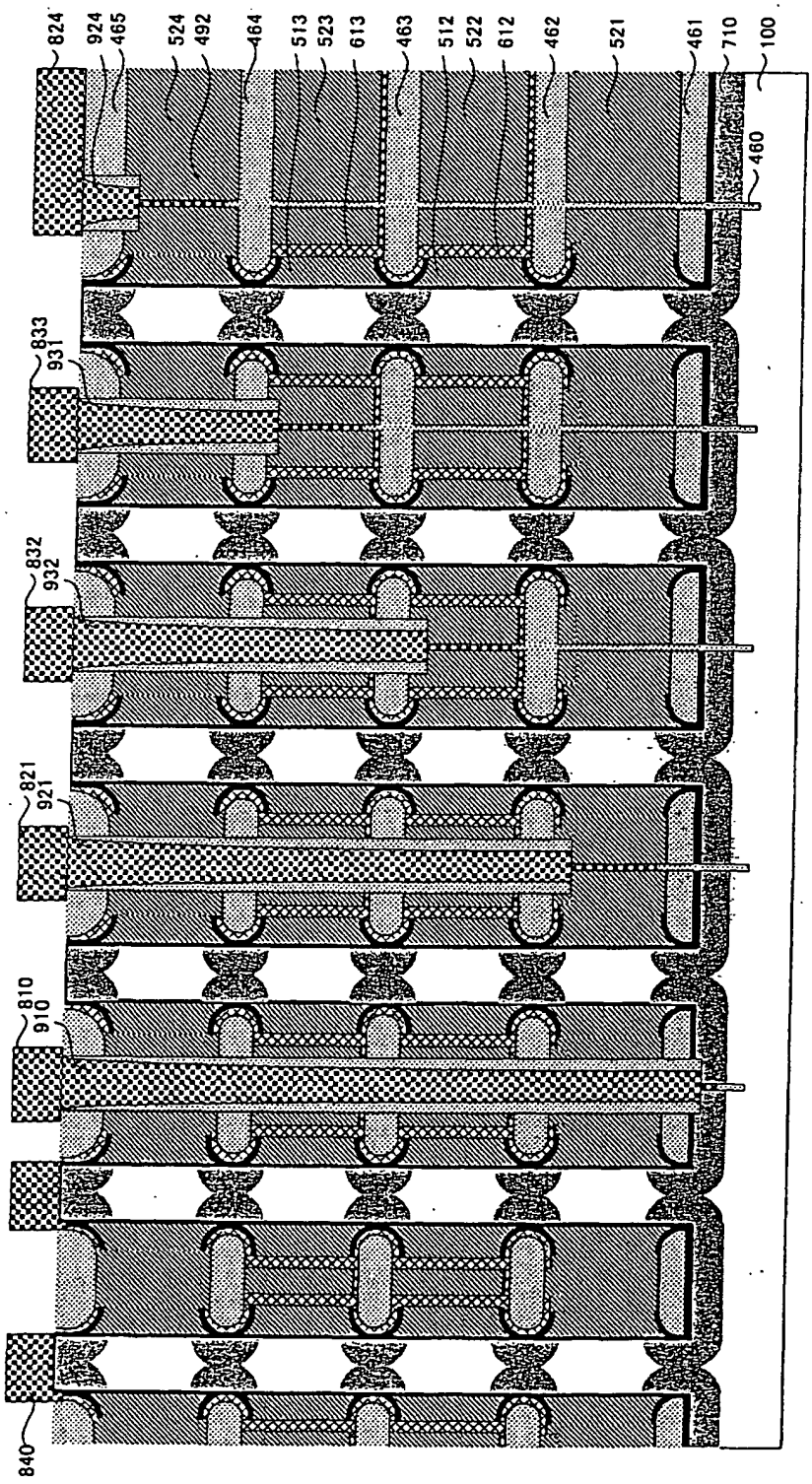
Fig. 794


824
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833
931
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Fig. 795

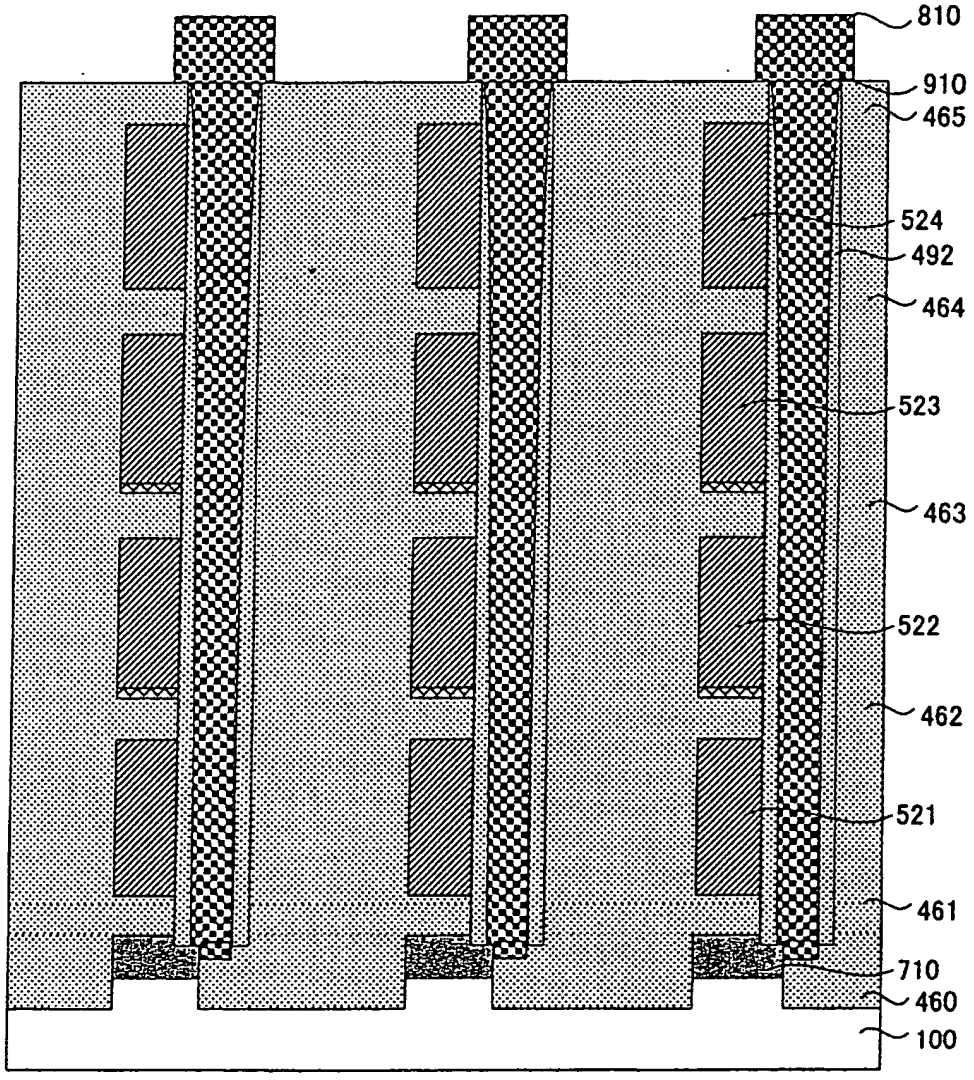

Fig. 796

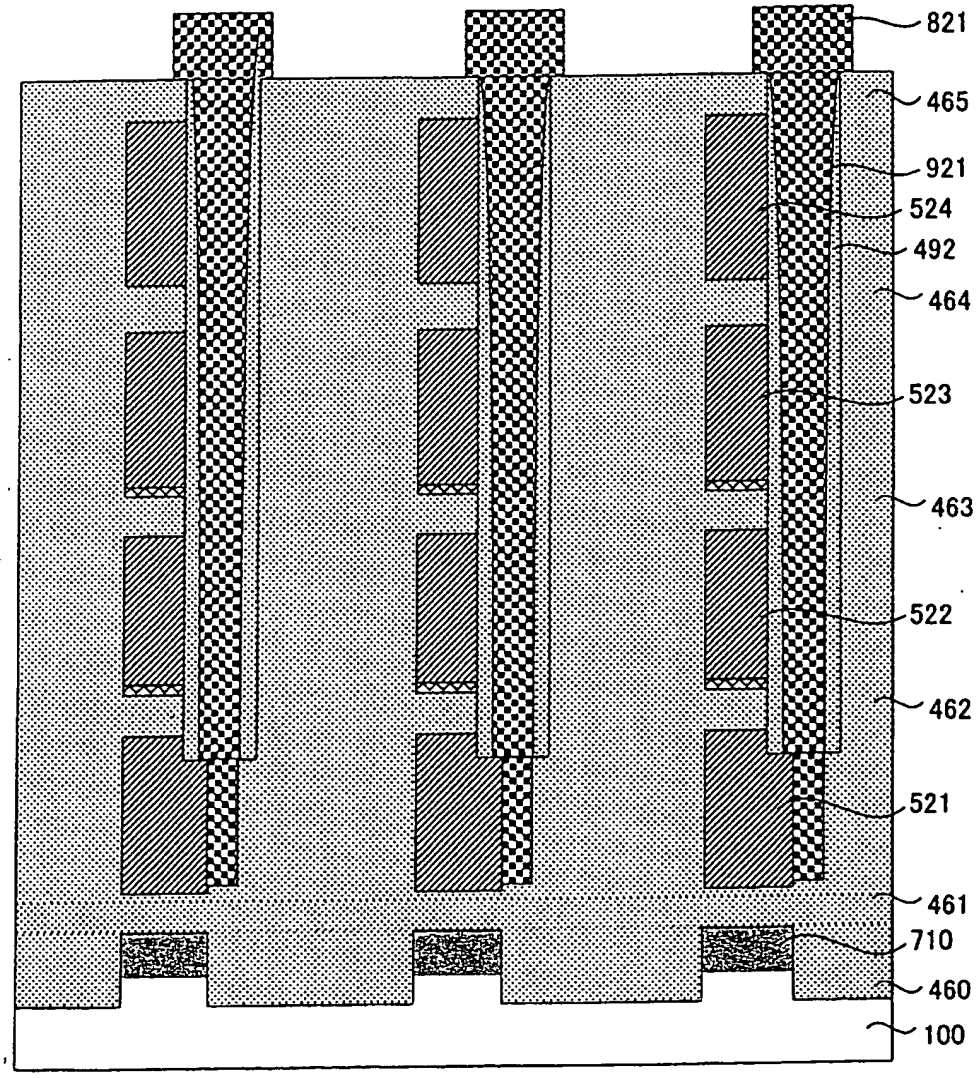

Fig. 797

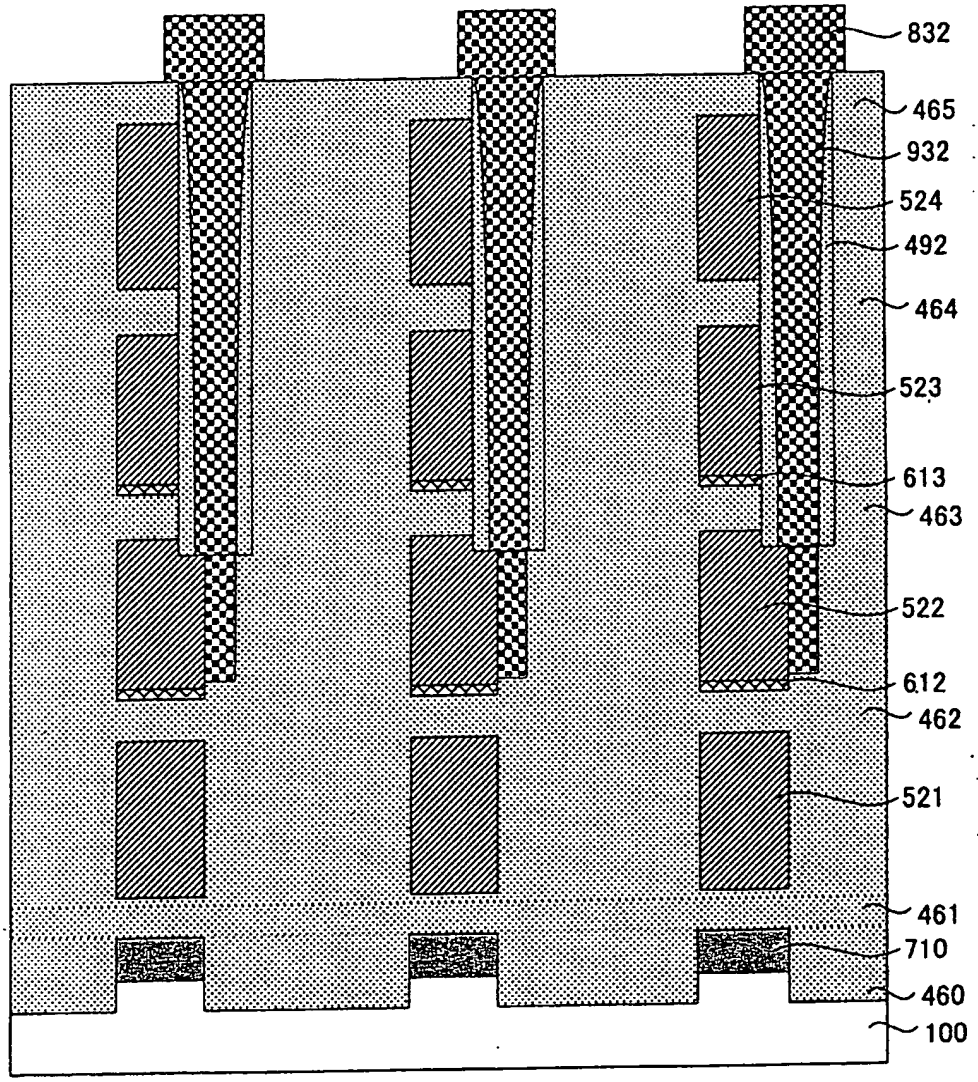
832
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Fig. 798

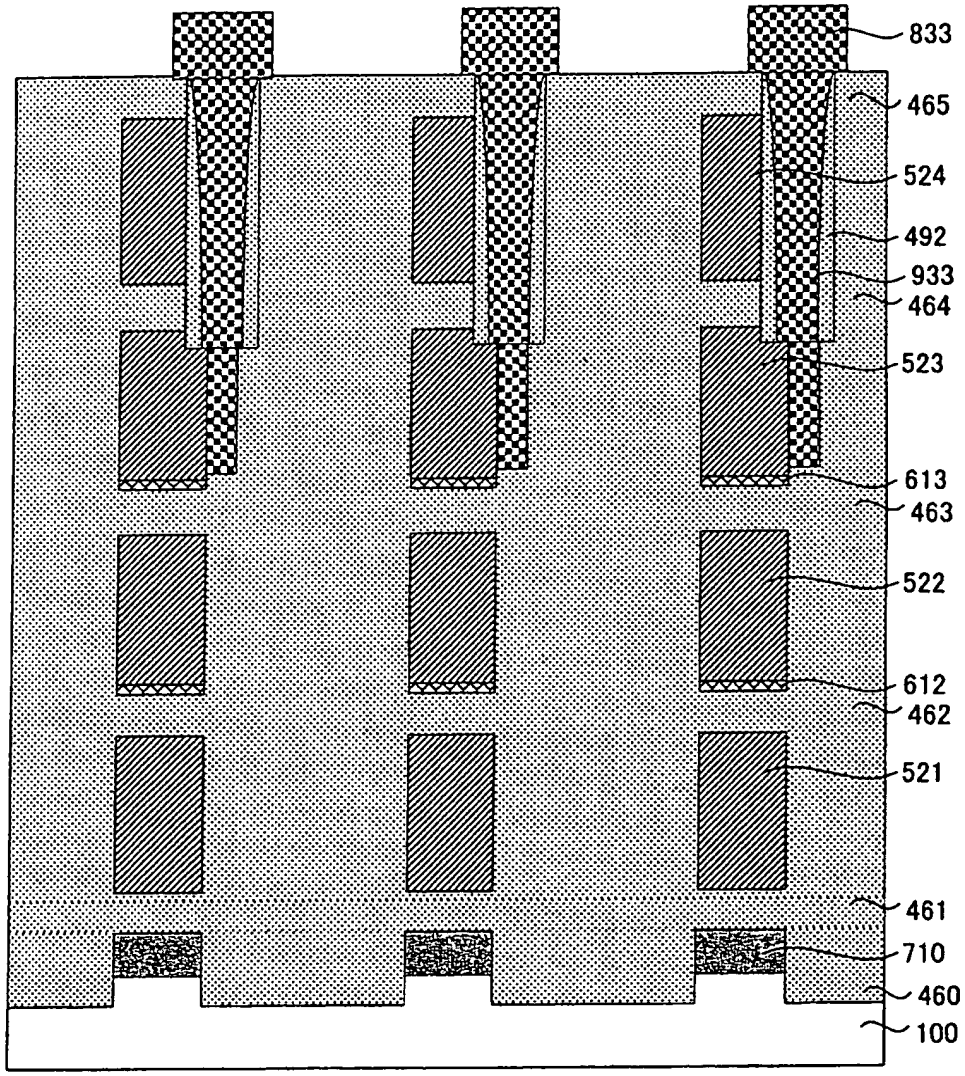
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Fig. 799

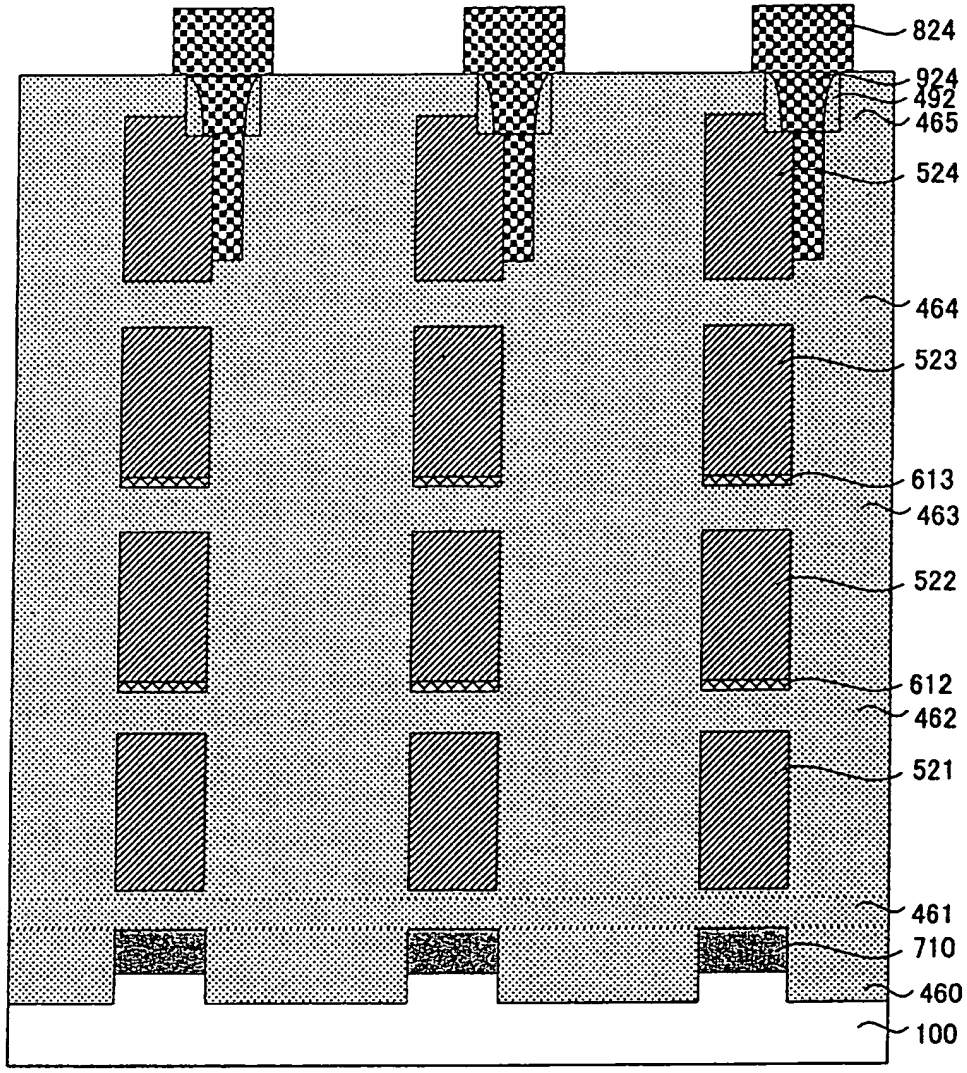
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Fig. 800 Prior Art

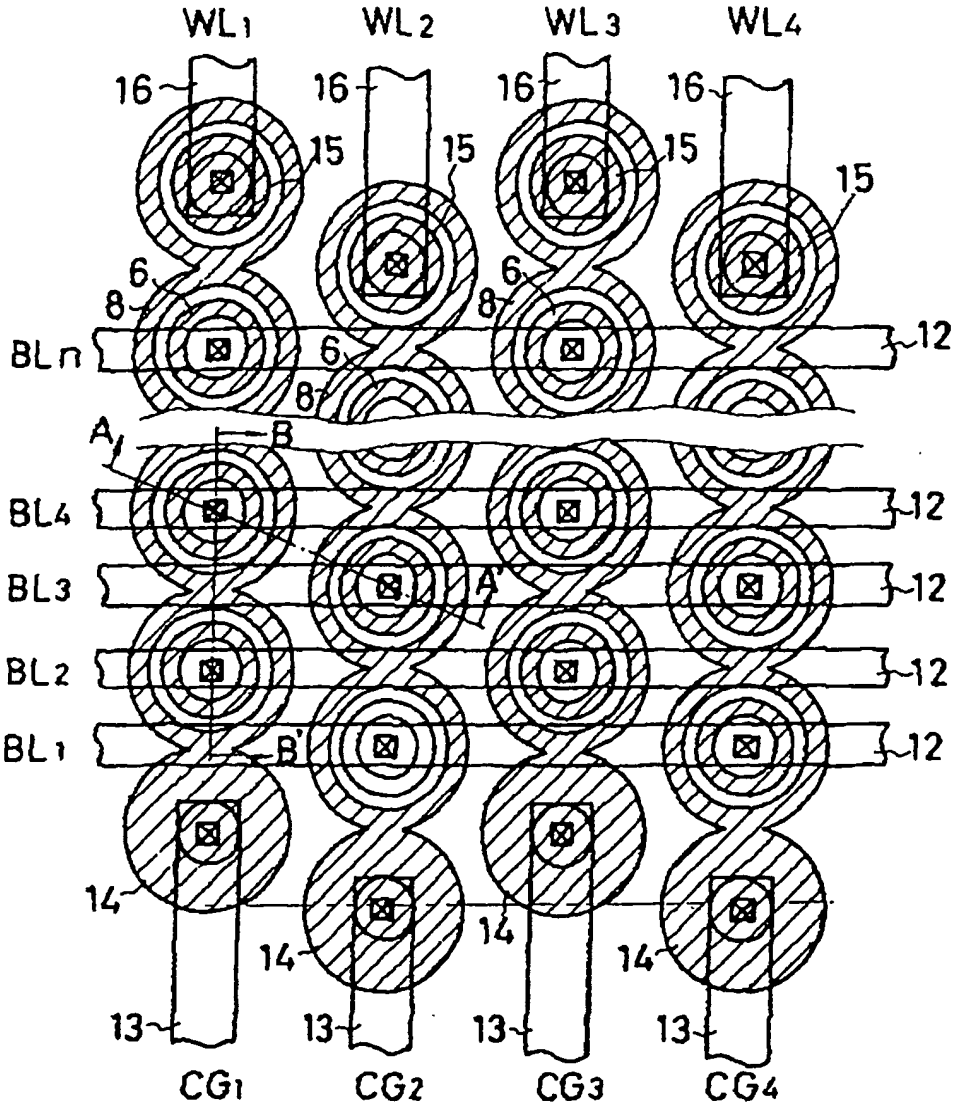

Fig. 801 (a)
Prior Art

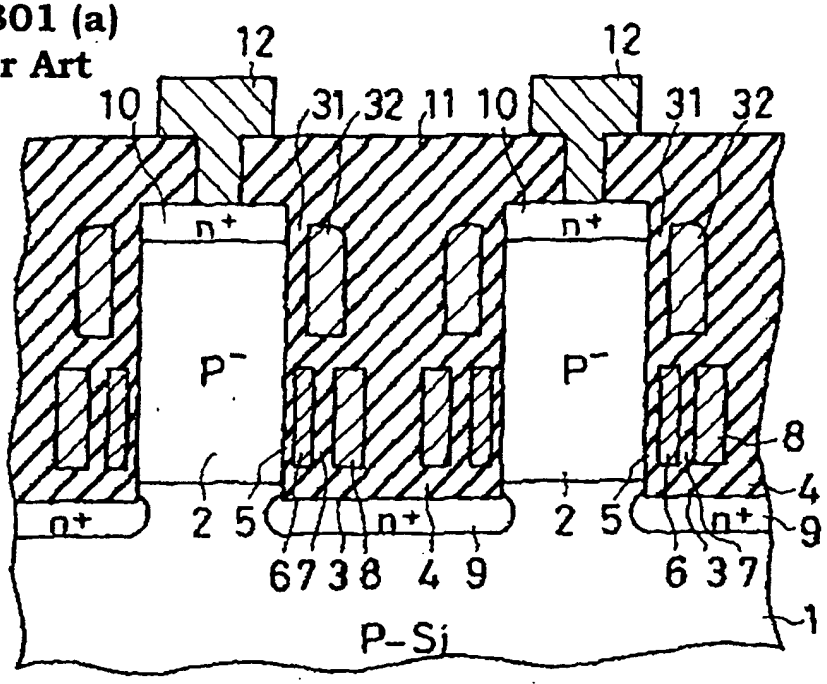


Fig. 801 (b)
Prior Art

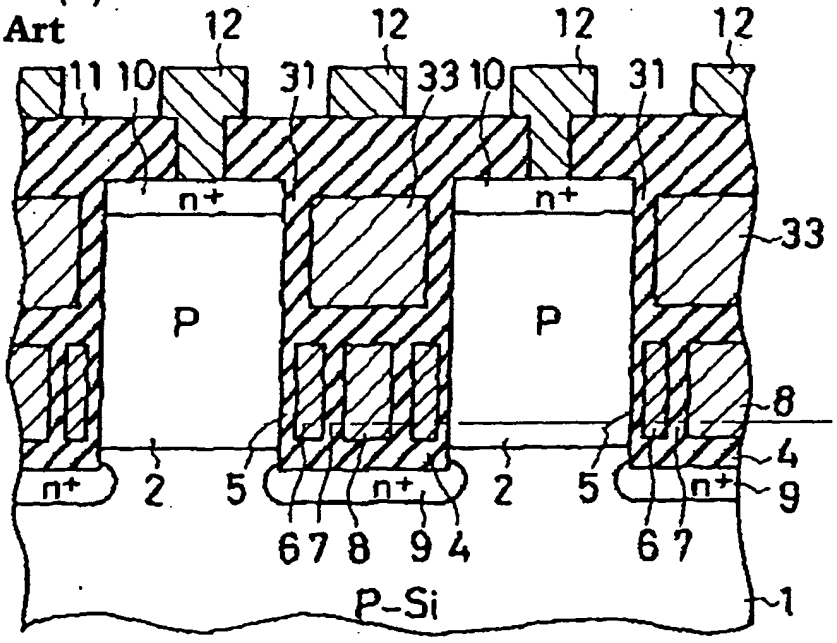

Fig. 802 (a)
Prior Art

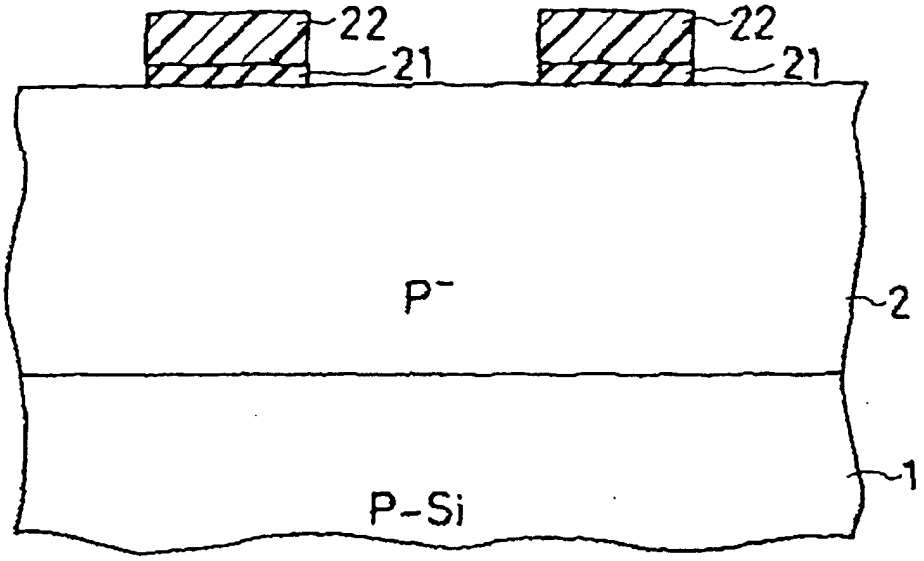


Fig. 802 (b)
Prior Art

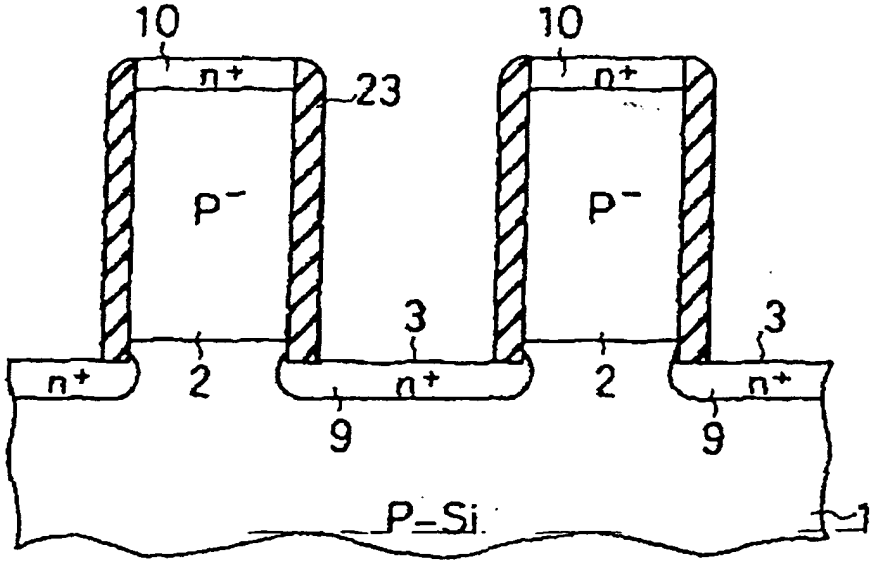

Fig. 803 (c)
Prior Art

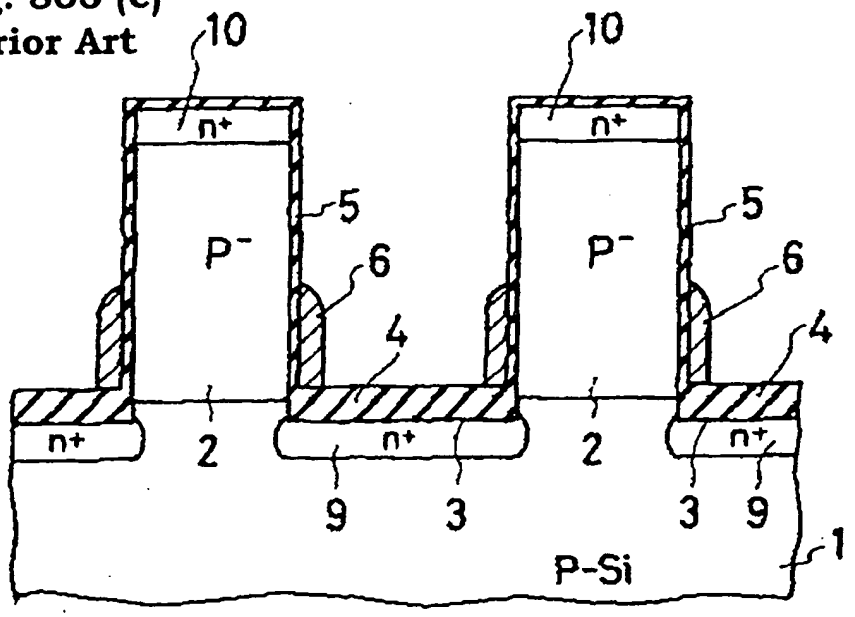


Fig. 803 (d)
Prior Art

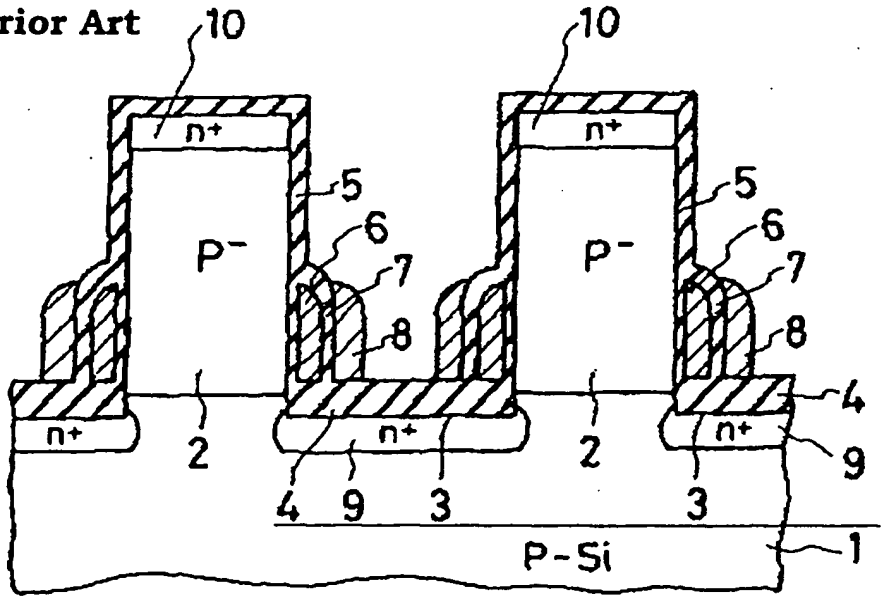

Fig. 804 (e)
Prior Art

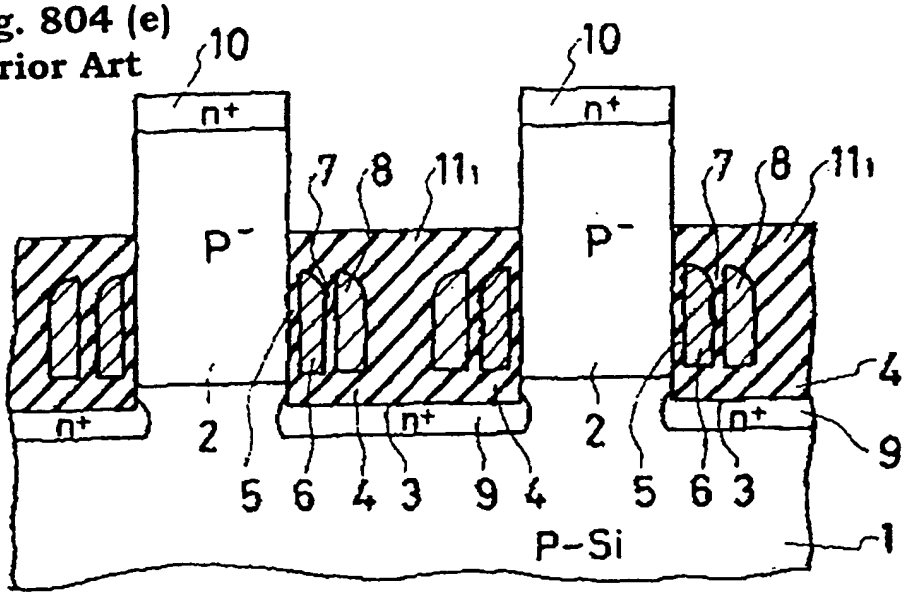


Fig. 804 (f)
Prior Art

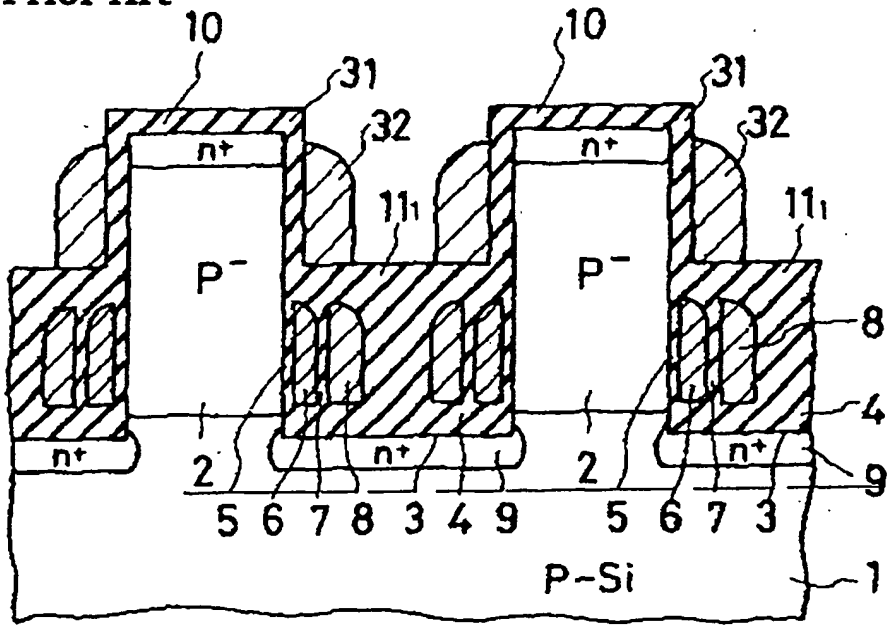

Fig. 805 (g)
Prior Art

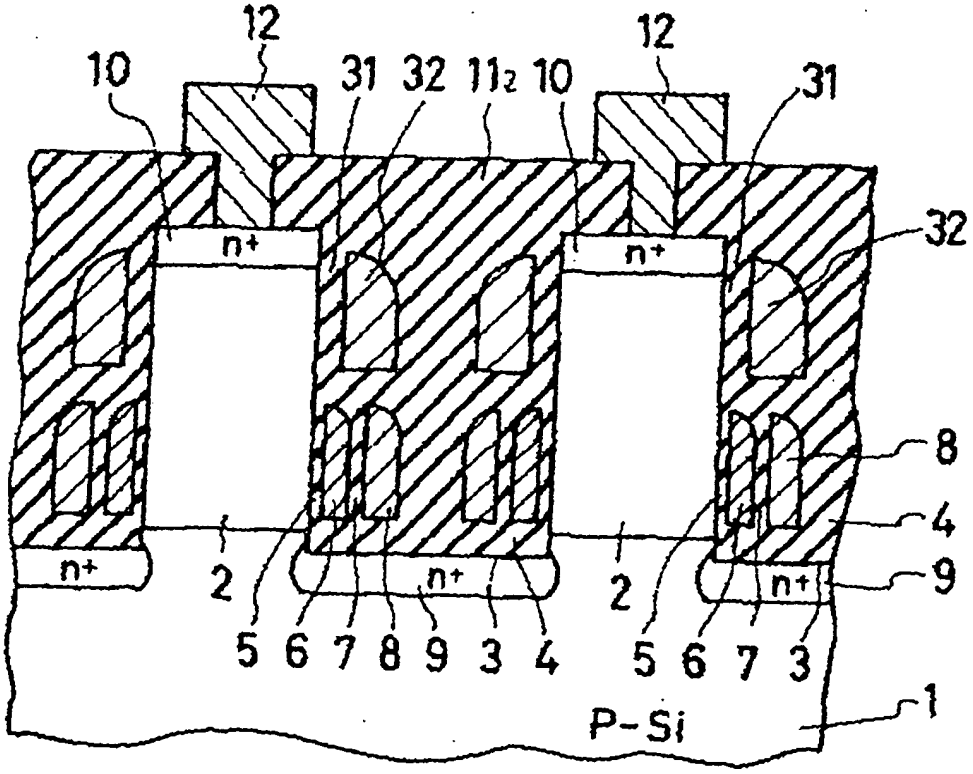

Fig. 806 (a)
Prior Art

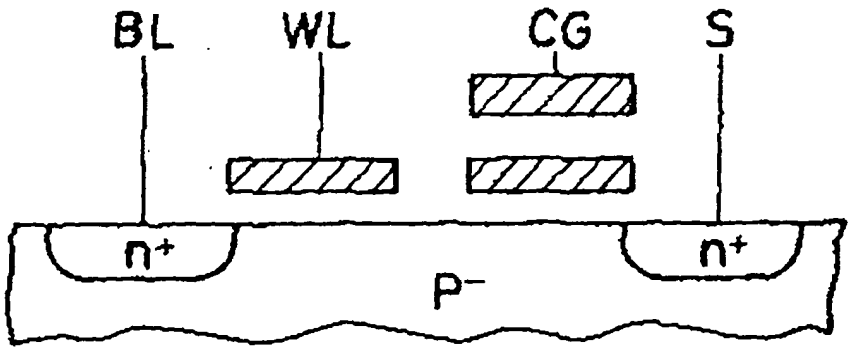


Fig. 806 (b)
Prior Art

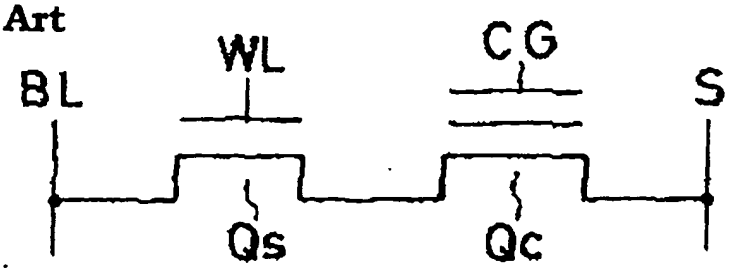

Fig. 807
Prior Art

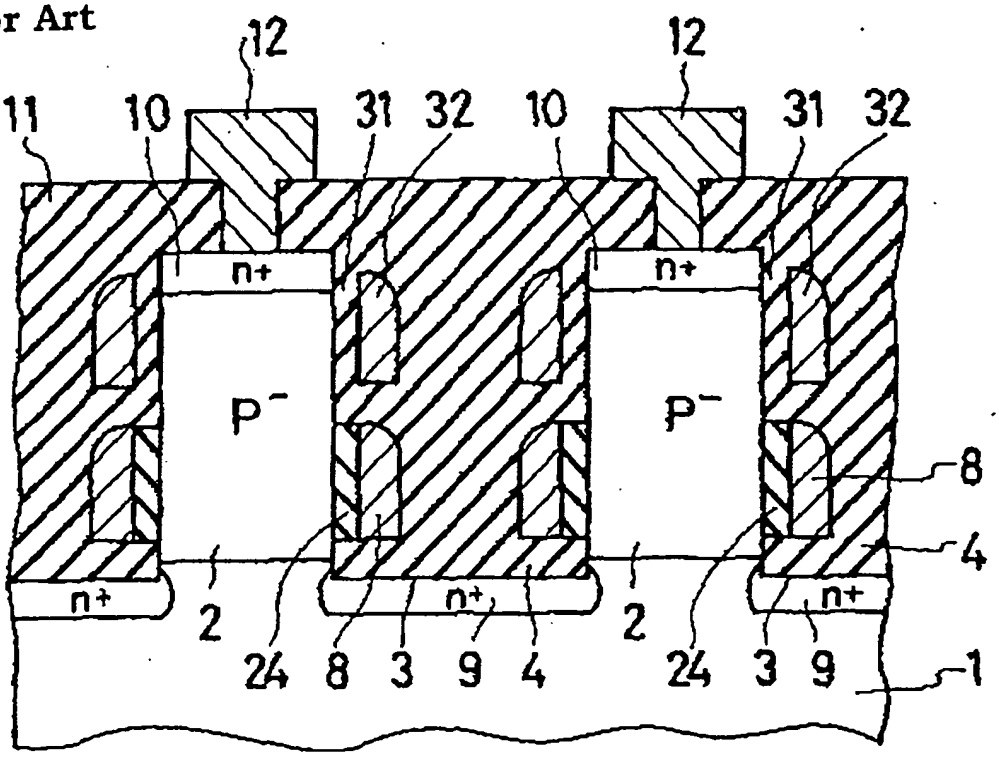

Fig. 808
Prior Art

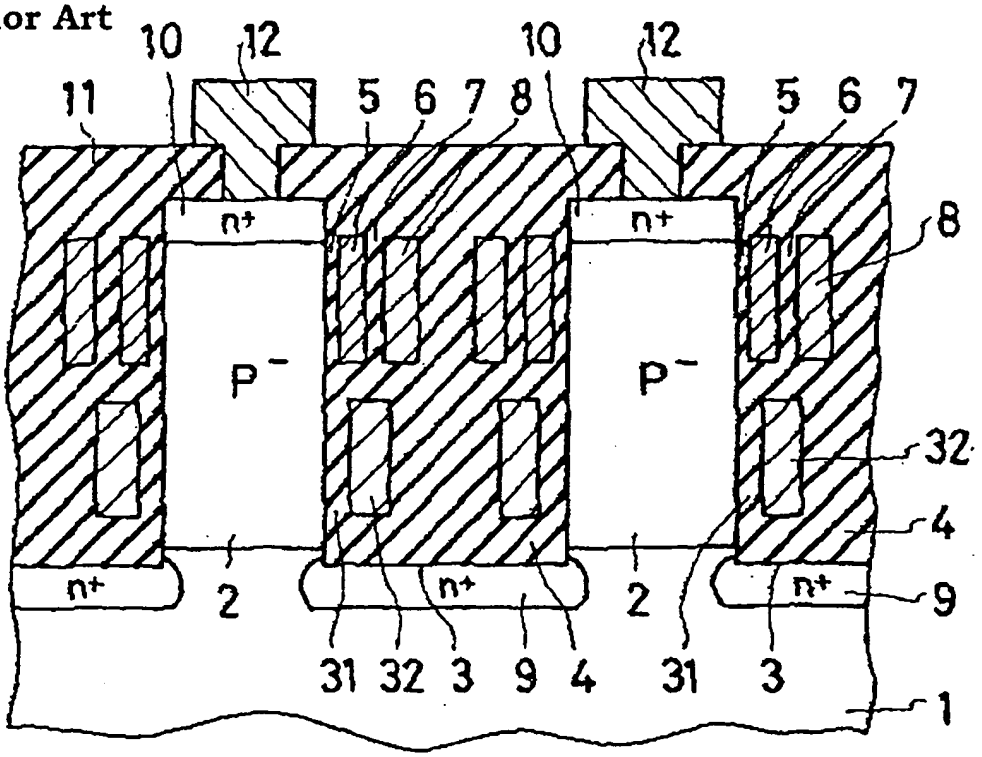

Fig. 809
Prior Art